UNIT IV – POWER DEVICES

UNI-JUNCTION TRANSISTOR

The UJT as the name implies, is characterized by a single pn junction. It exhibits negative resistance characteristic that makes it useful in oscillator circuits.

The symbol for UJT is shown in **fig.**i. The UJT is having three terminals base1 (B1), base2 (B2) and emitter (E). The UJT is made up of an N-type silicon bar which acts as the base as shown in **fig.** ii. It is very lightly doped. A P-type impurity is introduced into the base, producing a single PN junction called emitter. The PN junction exhibits the properties of a conventional diode.

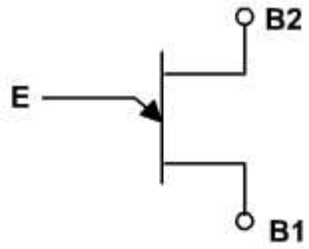


Fig. i

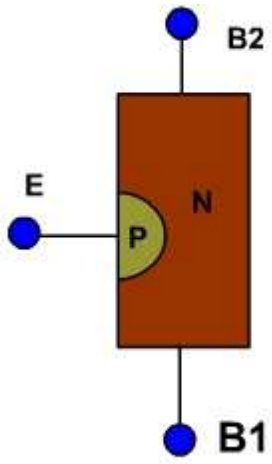


Fig .ii

A complementary UJT is formed by a P-type base and N-type emitter. Except for the polarity of voltage and current the characteristic is similar to those of a conventional UJT.

A simplified equivalent circuit for the UJT is shown in **fig.**iii . V_{BB} is a source of biasing voltage connected between B2 and B1. When the emitter is open, the total resistance from B2 to B1 is simply the resistance of the silicon bar, this is known as the inter base resistance R_{BB}. Since the N-channel is lightly doped, therefore R_{BB} is relatively high, typically 5 to 10K ohm. R_{B2} is the resistance between B2 and point ‘a', while R_{B1} is the resistance from point ‘a' to B1, therefore the interbase resistance R_{BB} is

$R_{BB} = R_{B1} + R_{B2}$

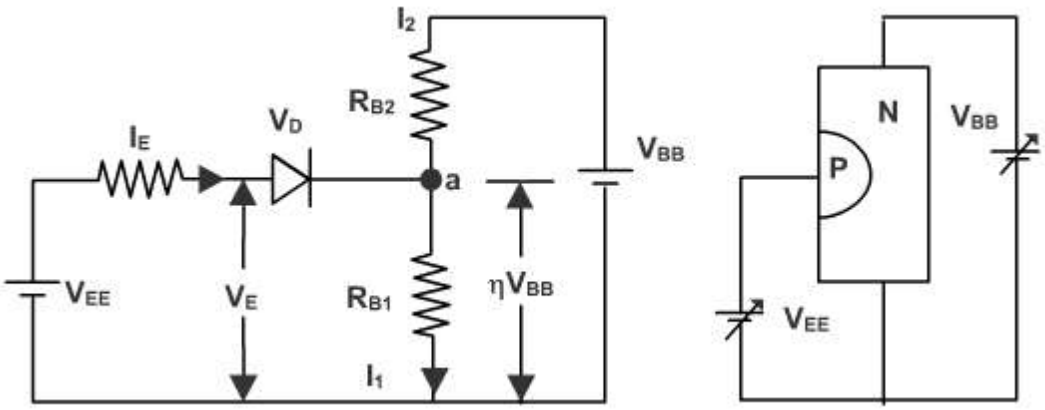


Fig.iii

The diode accounts for the rectifying properties of the PN junction. V_D is the diode's threshold voltage. With the emitter open, $I_E = 0$, and $I_1 = I_2$. The interbase current is given by

$I_1 = I_2 = V_{BB} / R_{BB}$.

Part of V_{BB} is dropped across R_{B2} while the rest of voltage is dropped across R_{B1}. The voltage across R_{B1} is

$V_a = V_{BB} * (R_{B1}) / (R_{B1} + R_{B2})$

The ratio $R_{B1} / (R_{B1} + R_{B2})$ is called intrinsic standoff ratio

$h = R_{B1} / (R_{B1} + R_{B2})$ i.e. $V_a = h V_{BB}$.

The ratio h is a property of UJT and it is always less than one and usually between 0.4 and 0.85. As long as $I_B = 0$, the circuit of behaves as a voltage divider.

Assume now that v_E is gradually increased from zero using an emitter supply V_{EE} . The diode remains reverse biased till v_E voltage is less than $h V_{BB}$ and no emitter current flows except leakage current. The emitter diode will be reversed biased.

When $v_E = V_D + h V_{BB}$, then appreciable emitter current begins to flow where V_D is the diode's threshold voltage. The value of v_E that causes, the diode to start conducting is called the peak point voltage and the current is called peak point current I_P.

$V_P = V_D + h\, V_{BB}$.

The graph of **fig. iv** shows the relationship between the emitter voltage and current. v_E is plotted on the vertical axis and I_E is plotted on the horizontal axis. The region from $v_E = 0$ to $v_E = V_P$ is called cut off region because no emitter current flows (except for leakage). Once v_E exceeds the peak point voltage, I_E increases, but v_E decreases. up to certain point called valley point (V_V and I_V). This is called negative resistance region. Beyond this, I_E increases with v_E this is the saturation region, which exhibits a positive resistance characteristic.

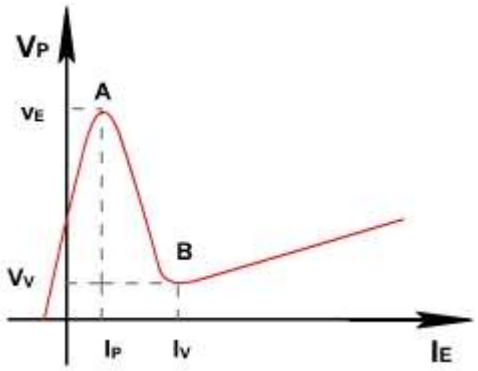


Fig. iv

The physical process responsible for the negative resistance characteristic is called conductivity modulation. When the v_E exceeds V_P voltage, holes from P emitter are injected into N base. Since the P region is heavily doped compared with the N-region, holes are injected to the lower half of the UJT.

The lightly doped N region gives these holes a long lifetime. These holes move towards B1 to complete their path by re-entering at the negative terminal of V_{EE}. The large holes create a conducting path between the emitter and the lower base. These increased charge carriers represent a decrease in resistance R_{B1}, therefore can be considered as variable resistance. It decreases up to 50 ohm.

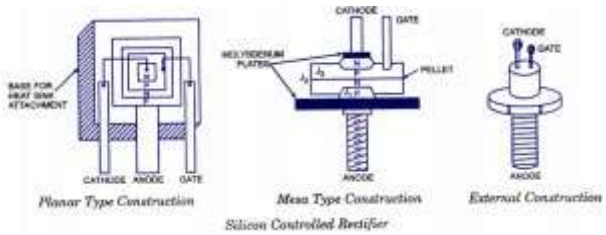
Since h is a function of R_{B1} it follows that the reduction of R_{B1} causes a corresponding reduction in intrinsic standoff ratio. Thus as I_E increases, R_{B1} decreases, h decreases, and V_a decreases. The decrease in V_a causes more emitter current to flow which causes further reduction in R_{B1}, h, and V_a. This process is regenerative and therefore V_a as well as v_E quickly drops while I_E increases. Although R_B decreases in value, but it is always positive resistance. It is only the dynamic resistance between V_V and V_P. At point B, the entire base1 region will saturate with carriers and resistance R_{B1} will not decrease any more. A further increase in I_e will be followed by a voltage rise.

The diode threshold voltage decreases with temperature and R_{BB} resistance increases with temperature because Si has positive temperature coefficient.

SILICON-CONTROLLED RECTIFIER

A Silicon-Controlled Rectifier (SCR) is a four-layer (p-n-p-n) semiconductor device that doesn't allow current to flow until it is triggered and, once triggered, will only allow the flow of current in one direction. It has three terminals: 1) an input control terminal referred to as a 'gate'; 2) an output terminal known as the 'anode'; and 3) a terminal known as a 'cathode', which is common to both the gate and the anode.

CONSTRUCTION OF AN SCR



SCR - construction types

From fig a it is clear that SCR is essentially an ordinary rectifier (PN) and a junction transistor (N-P-N) combined in one unit to form PNPN device. Three terminals are taken: one from the outer P-type material, known as anode, second from the outer N-type material, known as cathode and the third from the base of transistor section known as the gate.

The basic material used for fabrication of an SCR is N-type silicon. It has a specific resistance of about 6 ohm-mm. Silicon is the natural choice as base material because of the following advantages

(i) ability to withstand high junction temperature of the order of 150° C

(ii) high thermal conductivity;

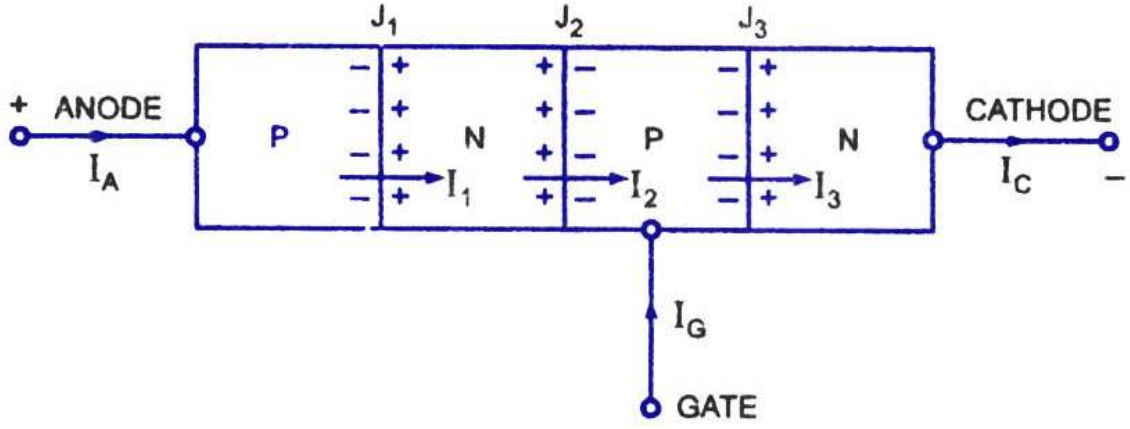
(iii) less variations in characteristics with temperature; and

(iv) less leakage current in P-N junction.

It consists, essentially, of a four layer pellet of P and N type silicon semiconductor materials. The junctions are diffused or alloyed. The material which may be used for P diffusion is aluminium and for N diffusion is phosphorous. The contact with anode can be made with an aluminium foil and through

cathode and gate by metal sheet. Diffusion must be carried out at a proper temperature and for necessary duration to provide correct concentration because this decides the properties of the device. Low power SCRs employ the planar construction shown in fig a. Planar construction is useful for making a number of units from a silicon wafer. Here, all the junctions are diffused. The other technique is the mesa construction shown in fig.b. This technique is used for high power SCRs. In this technique, the inner junction J_2 is obtained by diffusion, and then the outer two layers are alloyed to it. The PNPN pellet is properly braced with tungsten or molybdenum plates to provide greater mechanical strength and make it capable of handling large currents. One of these plates is hard soldered to a copper or an aluminium stud, which is threaded for attachment to a heat sink. This provides an efficient thermal path for conducting the internal losses to the surrounding medium. The uses of hard solder between the pellet and back-up plates minimises thermal fatigue, when the SCRs are subjected to temperature induced stresses. For medium and low power SCRs, the pellet is mounted directly on the copper stud or casing, using a soft solder which absorbs the thermal stresses set up by differential expansion and provides a good thermal path for heat transfer. For a larger cooling arrangement, which is required for high power SCRs, the press-pack or hockey-puck construction is employed, which provides for double-sided air for cooling.

Principle of Operation



The **SCR** is a four-layer, three-junction and a three-terminal device and is shown in fig.a. The end P-region is the anode, the end N-region is the cathode and the inner P-region is the gate. The anode to cathode is connected in series with the load circuit. Essentially the device is a switch. Ideally it remains off (voltage blocking state), or appears to have an infinite impedance until both the anode and gate terminals have suitable positive voltages with respect to the cathode terminal. The thyristor then switches on and current flows and continues to conduct without further gate signals. Ideally the thyristor has zero

impedance in conduction state. For switching off or reverting to the blocking state, there must be no gate signal and the anode current must be reduced to zero. Current can flow only in one direction.

In absence of external bias voltages, the majority carrier in each layer diffuses until there is a built-in voltage that retards further diffusion. Some majority carriers have enough energy to cross the barrier caused by the retarding electric field at each junction. These carriers then become minority carriers and can recombine with majority carriers. Minority carriers in each layer can be accelerated across each junction by the fixed field, but because of absence of external circuit in this case the sum of majority and minority carrier currents must be zero.

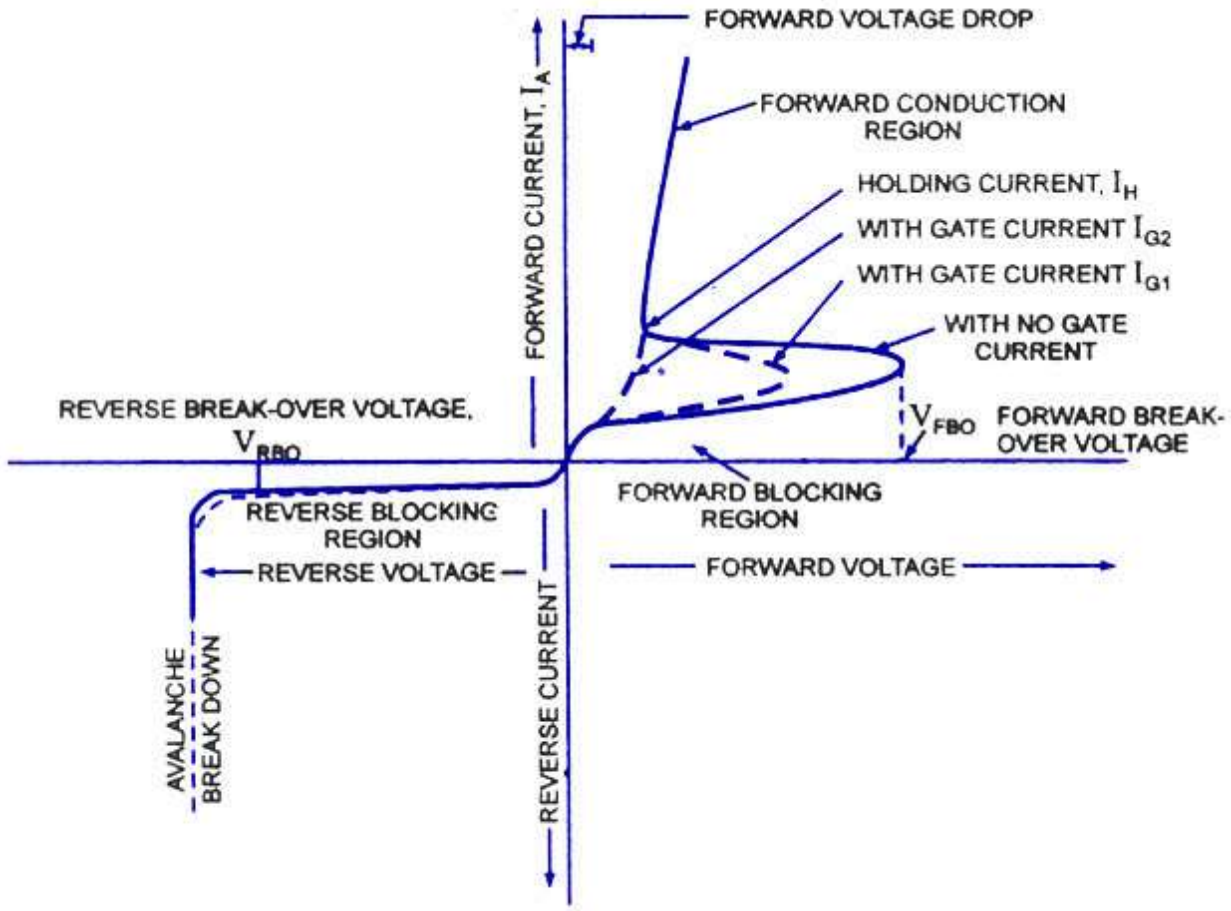
A voltage bias, as shown in figure, and an external circuit to carry current allow internal currents which include the following terms:

The current I_x is due to

- Majority carriers (holes) crossing junction J_1
- Minority carriers crossing junction J_1
- Holes injected at junction J_2 diffusing through the N-region and crossing junction J_1 and
- Minority carriers from junction J_2 diffusing through the N-region and crossing junction J_1.

Similarly I_2 is due to six terms and I_3 is due to four terms.

SCR Characteristics



V-I Characteristics of SCR

As already mentioned, the **SCR** is a four-layer device with three terminals, namely, the anode, the cathode and the gate. When the anode is made positive with respect to the cathode, junctions J_1 and J_3 are forward biased and junction J_2 is reverse-biased and only the leakage current will flow through the device. The SCR is then said to be in the forward blocking state or in the forward mode or off state. But when the cathode is made positive with respect to the anode, junctions J_1 and J_3 are reverse-biased, a small reverse leakage current will flow through the SCR and the SGR is said to be in the reverse blocking state or in reverse mode.

When the anode is positive with respect to cathode i.e. when the SCR is in forward mode, the SCR does not conduct unless the forward voltage exceeds certain value, called the forward breakover voltage, V_{FB0}. In non-conducting state, the current through the SCR is the leakage current which is very small and is

negligible. If a positive gate current is supplied, the SCR can become conducting at a voltage much lesser than forward break-over voltage. The larger the gate current, lower the break-over voltage. With sufficiently large gate current, the SCR behaves identical to PN rectifier. Once the SCR is switched on, the forward voltage drop across it is suddenly reduced to very small value, say about 1 volt. In the conducting or on-state, the current through the SCR is limited by the external impedance.

When the anode is negative with respect to cathode, that is when the SCR is in reverse mode or in blocking state no current flows through the SCR except very small leakage current of the order of few micro-amperes. But if the reverse voltage is increased beyond a certain value, called the reverse break-over voltage, $V_{\mathbf{RB0}}$ avalanche break down takes place. Forward break-over voltage $V_{\mathbf{FB0}}$ is usually higher than reverse breakover voltage,$\mathbf{V_{RBO}}$.

From the foregoing discussion, it can be seen that the SCR has two stable and reversible operating states. The change over from off-state to on-state, called turn-on, can be achieved by increasing the forward voltage beyond $\mathbf{V_{FB0}}$. A more convenient and useful method of turn-on the device employs the gate drive. If the forward voltage is less than the forward break-over voltage, V_{FB0}, it can be turned-on by applying a positive voltage between the gate and the cathode. This method is called the gate control. Another very important feature of the gate is that once the SCR is triggered to on-state the gate loses its control.

The switching action of gate takes place only when

(i) SCR is forward biased i.e. anode is positive with respect to cathode, and

(ii) Suitable positive voltage is applied between the gate and the cathode.

Once the SCR has been switched on, it has no control on the amount of current flowing through it. The current through the SCR is entirely controlled by the external impedance connected in the circuit and the applied voltage. There is, however, a very small, about 1 V, potential drop across the SCR. The forward current through the SCR can be reduced by reducing the applied voltage or by increasing the circuit impedance. There is, however, a minimum forward current that must be maintained to keep the SCR in conducting state. This is called the holding current rating of SCR. If the current through the SCR is reduced below the level of holding current, the device returns to off-state or blocking state.

The SCR can be switched off by reducing the forward current below the level of holding current which may be done either by reducing the applied voltage or by increasing the circuit impedance.

Note : The gate can only trigger or switch-on the SCR, it cannot switch off.

Alternatively the SCR can be switched off by applying negative voltage to the anode (reverse mode), the SCR naturally will be switched off.

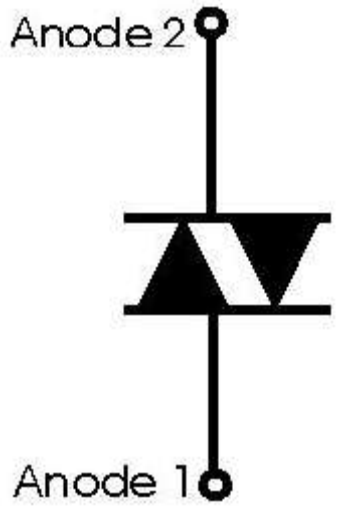
Here one point is worth mentioning, the SCR takes certain time to switch off. The time, called the turn-off time, must be allowed before forward voltage may be applied again otherwise the device will switch-on with forward voltage without any gate pulse. The turn-off time is about 15 micro-seconds, which is immaterial when dealing with power frequency, but this becomes important in the inverter circuits, which are to operate at high frequency.

Applications:

The six applications of SCR like power control, switching, zero-voltage switching, **over-voltage protection**, **pulse circuits** and battery charging regulator.

DIAC **DIAC (Diode for Alternating Current)**

Symbol



Construction:

The diac is basically a two terminal parellel-inverse combination of semiconductor layers that permits triggering in either direction. The basic arrangement of the semiconductor layers of the diac is shown in the figure, along with its graphical symbol. Nore that either terminal is referred as the cathode. Instead,

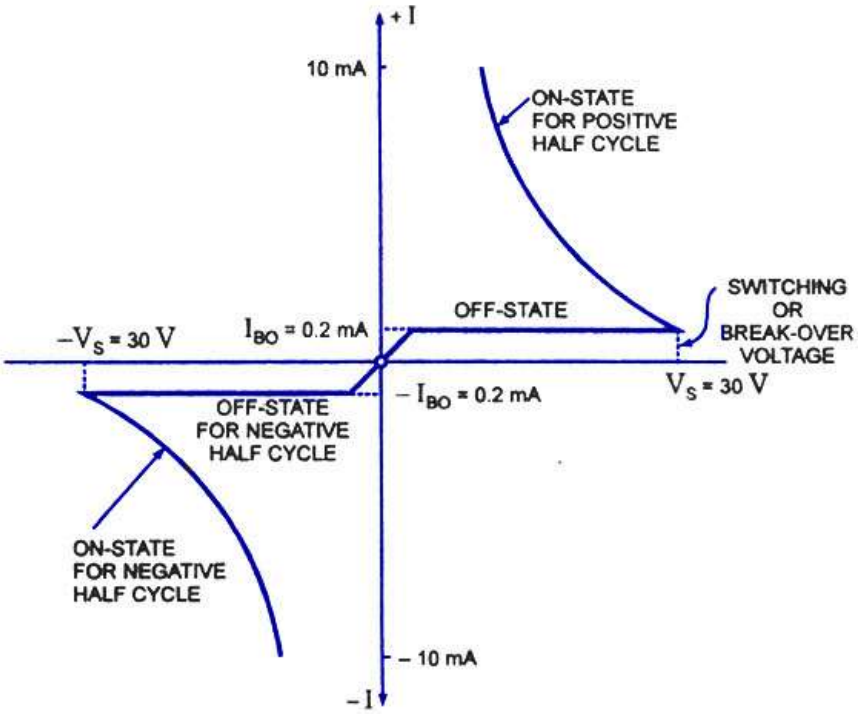
there is an anode 1 and an anode 2. When the anode 1 is positive with respect to anode 2, the semiconductor

Operation:

Diac circuits use the fact that a diac only conducts current only after a certain breakdown voltage has been exceeded. The actual breakdown voltage will depend upon the specification for the particular component type.

When the diac breakdown voltage occurs, the resistance of the component decreases abruptly and this leads to a sharp decrease in the voltage drop across the diac, and a corresponding increase in current. The diac will remain in its conducing state until the current flow through it drops below a particular value known as the holding current. When the current falls below the holding current, the diac switches back to its high resistance, or non-conducting state.
Diacs are widely used in AC applications and it is found that the device is "reset" to its non-conducting state, each time the voltage on the cycle falls so that the current falls below the holding current. As the behaviour of the device is approximately equal in both directions, it can provide a method of providing equal switching for both halves of an AC cycle, e.g for triacs.

Most diacs have a breakdown voltage of around 30 volts, although the exact specifications will depend upon the particular type of device.. Interestingly their behaviour is somewhat similar to that of a neon lamp, although they offer a far more precise switch on voltage and thereby provide a far better degree of switching equalization



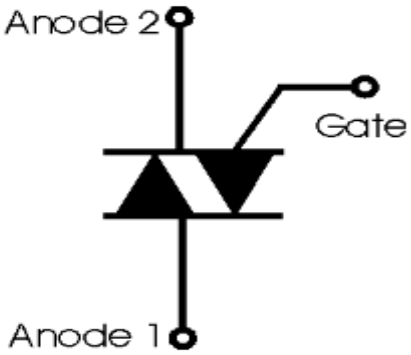
V-I Characteristic of a Diac

TRIAC (Triode for Alternating Current)

The triac is a three terminal semiconductor device for controlling current. It is effectively a development of the SCR or thyristor, but unlike the thyristor which is only able to conduct in one direction, the triac is a biriectional device. As such the triac is an ideal device to use for AC switching applications because it can control the current flow over both halves of an alternating cycle. A thyristor is only able to control them over one half of a cycle. During the remaining half no conduction occurs and accordingly only half the waveform can be utilised.

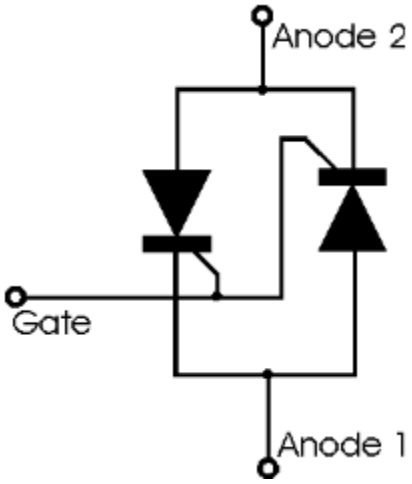
There are three terminal on a triac. These are the Gate and two other terminals. These other triac terminals are often referred to as an "Anode" or "Main Terminal"

TRIAC circuit symbol:



On the triac, the gate that acts as the trigger to turn the device on. The current then flows betweent he two anodes or main terminals. These are usually designated Anode 1 and Anode 2 or Main Terminal 1 and Main Terminal 2 (MT1 and MT2).

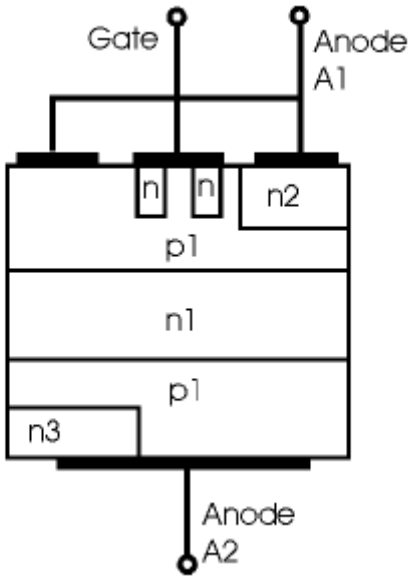
It can be imagined from the circuit symbol that the triac consists of two thyristors back to back. The operation of the triac can be looked on in this fashion, although the actual operation at the semiconductor level is rather complicated. When the voltage on the MT1 is positive with regard to MT2 and a positive gate voltage is applied, one of the SCRs conducts. When the voltage is reversed and a negative voltage is applied to the gate, the other SCR conducts. This is provided that there is sufficient voltage across the device to enable a minimum holding current to flow.



TRIAC OPERATION

The structure of a triac may be considered as a p-n-p-n structure and the triac may be considered to consist of two conventional SCRs fabricated in an inverse parallel configuration.

In operation, when terminal A2 is positive with respect to A1, then a positive gate voltage will give rise to a current that will trigger the part of the triac consisting of p1 n1 p2 n2 and it will have an identical characteristic to an SCR. When terminal A2 is negative with respect to A1 a negative current will trigger the part of the triac consisting of p2 n1 p1 n3. In this way conduction on the triac occurs over both halves an alternating cycle.



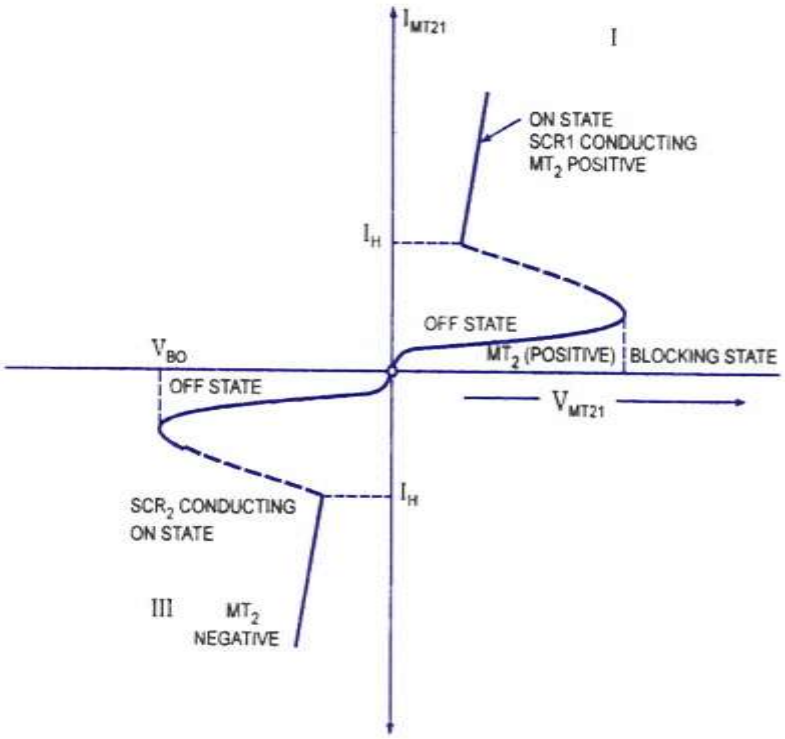
TRIAC structure

Triacs do not fire symmetrically as a result of slight differences between the two halves of the device. This results in harmonics being generated, and the less symmetrical the triac fires, the greater the level of harmonics produced. It is generally undesirable to have high levels of harmonics in a power system and as a result triacs are not favoured for high power systems. Instead two thyristors may be used as it is easier to control their firing.

To help in overcoming this problem, a device known as a diac (diode AC switch) is often placed in series with the gate. This device helps make the switching more even for both halves of the cycle. This results from the fact that the diac switching characteristic is far more even than that of the triac. Since the diac prevents any gate current flowing until the trigger voltage has reached a certain voltage in either direction, this makes the firing point of the triac more even in both directions.

Characteristics of TRIAC

Typical V-I characteristics of a triac are shown in figure. The triac has on and off state characteristics similar to SCR but now the char acteristic is applicable to both positive and negative voltages. This is expected because triac consists of two SCRs connected in parallel but opposite in directions.



V-I Characteristic of a Triac

MT_2 is positive with respect to MTX in the first quadrant and it is negative in the third quad rant. As already said in previous blog posts, the gate triggering may occur in any of the following four modes.

- Quadrant I operation : V_{MT2}, positive; V_{G1} positive
- Quadrant II operation : V_{MT21} positive; V_{Gl} negative
- Quadrant III operation : V_{MT21} negative; V_{Gl} negative
- Quadrant IV operation : V_{MT21} negative; V_{G1} positive

Where V_{MT21} and V_{Gl} are the voltages of terminal MT_2 and gate with respect to terminal MT_1.

- The device, when starts conduction permits a very heavy amount of current to flow through it. This large inrush of current must be restricted by employing external resist ance, otherwise the device may get damaged.
- The gate is the control terminal of the device. By applying proper signal to the gate, the firing angle of the device can be controlled.
- The circuits used in the gate for triggering the device are called the gate-triggering circuits. The gate-triggering circuits for the triac are almost same like those used for SCRs.
- These triggering circuits usually generate trigger pulses for firing the device. The trigger pulse should be of sufficient magnitude and duration so that firing of the device is assured. Usually, a duration of 35 us is sufficient for sustaining the firing of the device.

Application of TRIAC

- Low power TRIACs are used in many applications such as light dimmers, speed controls for electric fans and other electric motors, and in the modern computerized control circuits of many household small and major appliances.
- However, when used with inductive loads such as electric fans, care must be taken to assure that the TRIAC will turn off correctly at the end of each half-cycle of the AC power. Indeed, TRIACs can be very sensitive to high values of dv/dt between A1 and A2, so a phase shift between current and voltage (as in the case of an inductive load) leads to sudden voltage step which can make the device turn on in an unwanted manner.
- Unwanted turn-ons can be avoided by using a snubber circuit (usually of the RC or RCL type) between A1 and A2. Snubber circuits are also used to prevent premature triggering, caused for example by voltage spikes in the mains supply.
- Because turn-ons are caused by internal capacitive currents flowing into the gate as a consequence of a high voltage dv/dt, a gate resistor or capacitor (or both in parallel) may be connected between gate and A1 to provide a low-impedance path to A1 and further prevent false triggering. This, however, increases the required trigger current or adds latency due to capacitor charging. On the other hand, a resistor between the gate and A1 helps dragging leakage currents out of the device, thus improving the performance of the TRIAC at high temperature, where the maximum allowed dv/dt is lower. Values of resistors less than 1kΩ and capacitors of 100nF are generally suitable for this purpose, although the fine-tuning should be done on the particular device model.
- For higher-powered, more-demanding loads, two SCRs in inverse parallel may be used instead of one TRIAC. Because each SCR will have an entire half-cycle of reverse polarity voltage applied

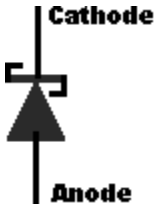
to it, turn-off of the SCRs is assured, no matter what the character of the load. However, due to the separate gates, proper triggering of the SCRs is more complex than triggering a TRIAC.

- In addition to commutation, a TRIAC may also not turn on reliably with non-resistive loads if the phase shift of the current prevents achieving holding current at trigger time. To overcome that, pulse trains may be used to repeatedly try to trigger the TRIAC until it finally turns on. The advantage is that the gate current does not need to be maintained throughout the entire conduction angle, which can be beneficial when there is only limited drive capability available.

SCHOTTKY BARRIER DIODE

- Schottky-barrier diode referred to as a surface-barrier, or hot-carrier diode .
- Its areas of application were first limited to the very high frequency range due to its quick response time and a lower noise figure . In recent years, however, it is appearing more and more in low-voltage/high-current power supplies and ac-to-dc converters.
- The other applications include radar systems, Schottky TTL logic for computers, mixers and detectors in communication equipment, instrumentation, and analog-to-digital converters

The symbol is as shown below.

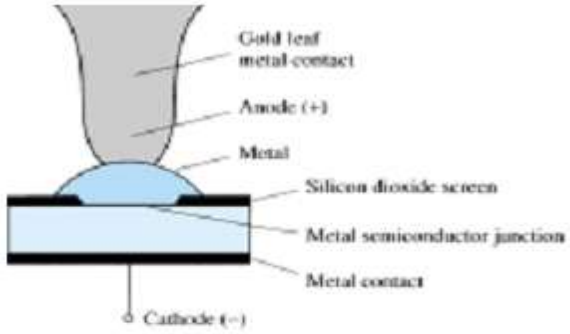


Construction

Its construction is quite different from the conventional p-n junction in that a metal semiconductor junction is created such as shown below. The semiconductor is normally n-type silicon (although p-type silicon is sometimes used), while a host of different metals, such as molybdenum, platinum, chrome, or tungsten, are used.

Different construction techniques will result in a different set of characteristics for the device, such as increased frequency range, lower forward bias, and so on.

Priorities do not permit an examination of each technique here, but information will usually be provided by the manufacturer. In general, however, Schottky diode construction results in a more uniform junction region and a high level of ruggedness. In both materials, the electron is the majority carrier. In the metal, the level of minority carriers (holes) is insignificant. When the materials are joined, the electrons in the n-type silicon semiconductor material immediately flow into the adjoining metal, establishing a heavy flow of majority carriers. Since the injected carriers have a very high kinetic energy level compared to the electrons of the metal, they are commonly called "hot carriers." In the conventional p-n junction, there was the injection of minority carriers into the adjoining region. Here the electrons are injected into a region of the same electron plurality. Schottky diodes are therefore unique in that conduction is entirely by majority carriers. The heavy flow of electrons into the metal creates a region near the junction surface depleted of carriers in the silicon material much like the depletion region in the p-n junction diode. The additional carriers in the metal establish a "negative wall" in the metal at the boundary between the two materials. The net result is a "surface barrier" between the two materials, preventing any further current. That is, any electrons (negatively charged) in the silicon material face a carrier-free region and a "negative wall" at the surface of the metal.



PRINCIPLE OF OPERATION AND CHARACTERISTICS

The application of a forward bias as shown in the first quadrant of Fig. 3 will reduce the strength of the negative barrier through the attraction of the applied positive potential for electrons from this region. The result is a return to the heavy flow of electrons across the boundary, the magnitude of which is controlled by the level of the applied bias potential. The barrier at the junction for a Schottky diode is less than that of the p-n junction device in both the

forward- and reverse-bias regions. The result is therefore a higher current at the same applied bias in the forward- and reverse-bias regions. This is a desirable effect in the forward-bias region but highly undesirable in the reverse-bias region

Circuit symbol

The Schottky circuit symbol used in many circuit schematic diagrams may be that of an ordinary diode symbol. However it is often necessary to use a specific Schottky diode symbol to signify that a Schottky diode rather than another one must be used because it is essential to the operation of the circuit. Accordingly a specific Schottky diode symbol has been accepted for use. The circuit symbol is shown in Fig.1.

Advantages

Schottky diodes are used in many applications where other types of diode will not perform as well. They offer a number of advantages:

- ***Low turn on voltage:*** The turn on voltage for the diode is between 0.2 and 0.3 volts for a silicon diode against 0.6 to 0.7 volts for a standard silicon diode. This makes it have very much the same turn on voltage as a germanium diode.
- ***Fast recovery time:*** The fast recovery time because of the small amount of stored charge means that it can be used for high speed switching applications.
- ***Low junction capacitance:*** In view of the very small active area, often as a result of using a wire point contact onto the silicon, the capacitance levels are very small.

The advantages of the Schottky diode, mean that its performance can far exceed that of other diodes in many areas.

Applications

The Schottky barrier diodes are widely used in the electronics industry finding many uses as diode rectifier. Its unique properties enable it to be used in a number of applications where other

diodes would not be able to provide the same level of performance. In particular it is used in areas including:

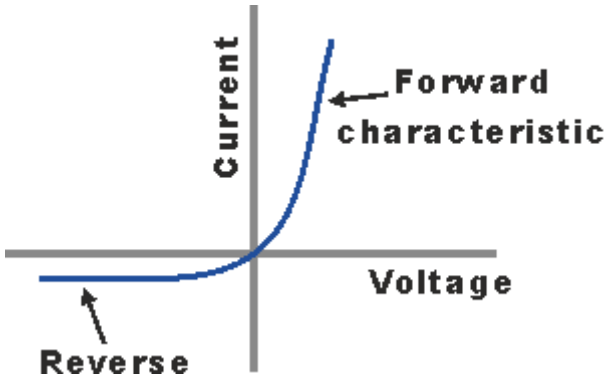
- ***RF mixer and detector diode***: The Schottky diode has come into its own for radio frequency applications because of its high switching speed and high frequency capability. In view of this Schottky barrier diodes are used in many high performance diode ring mixers. In addition to this their low turn on voltage and high frequency capability and low capacitance make them ideal as RF detectors.
- ***Power rectifier:*** Schottky barrier diodes are also used in high power applications, as rectifiers. Their high current density and low forward voltage drop mean that less power is wasted than if ordinary PN junction diodes were used. This increase in efficiency means that less heat has to be dissipated, and smaller heat sinks may be able to be incorporated in the design.
- ***Power OR circuits:*** Schottky diodes can be used in applications where a load is driven by two separate power supplies. One example may be a mains power supply and a battery supply. In these instances it is necessary that the power from one supply does not enter the other. This can be achieved using diodes. However it is important that any voltage drop across the diodes is minimised to ensure maximum efficiency. As in many other applications, this diode is ideal for this in view of its low forward voltage drop.

  Schottky diodes tend to have a high reverse leakage current. This can lead to problems with any sensing circuits that may be in use. Leakage paths into high impedance circuits can give rise to false readings. This must therefore be accommodated in the circuit design.
- ***Solar cell applications:*** Solar cells are typically connected to rechargeable batteries, often lead acid batteries because power may be required 24 hours a day and the Sun is not always available. Solar cells do not like the reverse charge applied and therefore a diode is required in series with the solar cells. Any voltage drop will result in a reduction in efficiency and therefore a low voltage drop diode is needed. As in other applications, the low voltage drop of the Schottky diode is particularly useful, and as a result they are the favoured form of diode in this application.

- ***Clamp diode - especially with its use in LS TTL:*** Schottky barrier diodes may also be used as a clamp diode in a transistor circuit to speed the operation when used as a switch. They were used in this role in the 74LS (low power Schottky) and 74S (Schottky) families of logic circuits. In these chips the diodes are inserted between the collector and base of the driver transistor to act as a clamp. To produce a low or logic "0" output the transistor is driven hard on, and in this situation the base collector junction in the diode is forward biased. When the Schottky diode is present this takes most of the current and allows the turn off time of the transistor to be greatly reduced, thereby improving the speed of the circuit.

Schottky diode IV characteristic

The IV characteristic is generally that shown below. In the forward direction the current rises exponentially, having a knee or turn on voltage of around 0.2 V. In the reverse direction, there is a greater level of reverse current than that experienced using a more conventional PN junction diode.



Schottky diode IV characteristic

The use of a guard ring in the fabrication of the diode has an effect on its performance in both forward and reverse directions. [see page on structure and fabrication]. Both forward and reverse characteristics show a better level of performance.

However the main advantage of incorporating a guard ring into the structure is to improve the reverse breakdown characteristic. There is around a 4 : 1 difference in breakdown voltage

between the two - the guard ring providing a distinct improvement in reverse breakdown. Some small signal diodes without a guard ring may have a reverse breakdown of only 5 to 10 V.

Key specification parameters

In view of the particular properties of the Schottky diode there are several parameters that are of key importance when determining the operation of one of these diodes against the more normal PN junction diodes.

- ***Forward voltage drop:*** In view of the low forward voltage drop across the diode, this is a parameter that is of particular concern. As can be seen from the Schottky diode IV characteristic, the voltage across the diode varies according to the current being carried. Accordingly any specification given provides the forward voltage drop for a given current. Typically the turn-on voltage is assumed to be around 0.2 V.
- ***Reverse breakdown:*** Schottky diodes do not have a high breakdown voltage. Figures relating to this include the maximum Peak Reverse Voltage, maximum Blocking DC Voltage and other similar parameter names. If these figures are exceeded then there is a possibility the diode will enter reverse breakdown. It should be noted that the RMS value for any voltage will be $1/\sqrt{2}$ times the constant value. The upper limit for reverse breakdown is not high when compared to normal PN junction diodes. Maximum figures, even for rectifier diodes only reach around 100 V. Schottky diode rectifiers seldom exceed this value because devices that would operate above this value even by moderate amounts would exhibit forward voltages equal to or greater than equivalent PN junction rectifiers.
- ***Capacitance:*** The capacitance parameter is one of great importance for small signal RF applications. Normally the junctions areas of Schottky diodes are small and therefore the capacitance is small. Typical values of a few picofarads are normal. As the capacitance is dependent upon any depletion areas, etc, the capacitance must be specified at a given voltage.
- ***Reverse recovery time:*** This parameter is important when a diode is used in a switching application. It is the time taken to switch the diode from its forward conducting or 'ON' state to the reverse 'OFF' state. The charge that flows within this time is referred to as the

'reverse recovery charge'. The time for this parameter for a Schottky diode is normally measured in nanoseconds, ns. Some exhibit times of 100 ps. In fact what little recovery time is required mainly arises from the capacitance rather than the majority carrier recombination. As a result there is very little reverse current overshoot when switching from the forward conducting state to the reverse blocking state.

- ***Working temperature:*** The maximum working temperature of the junction, Tj is normally limited to between 125 to 175°C. This is less than that which can be sued with ordinary silicon diodes. Care should be taken to ensure heatsinking of power diodes does not allow this figure to be exceeded.
- ***Reverse leakage current:*** The reverse leakage parameter can be an issue with Schottky diodes. It is found that increasing temperature significantly increases the reverse leakage current parameter. Typically for every 25°C increase in the diode junction temperature there is an increase in reverse current of an order of magnitude for the same level of reverse bias.

RECTIFIERS AND POWER SUPPLIES:

RECTIFIERS

Diodes are referred to as non-linear circuit elements because of the above characteristic curve. For most applications the non-linear region can be avoided and the device can be modeled by piece-wise linear circuit elements. Qualitatively we can just think of an ideal diode has having two regions: a conduction region of zero resistance and an infinite resistance non-conduction region. For many circuit applications, this ideal diode model is an adequate representation of an actual diode and simply requires that the circuit analysis be separated into two parts: forward current and reverse current. Figure 5.1 shows a schematic symbol for a diode and the current-voltage curve for an ideal diode.

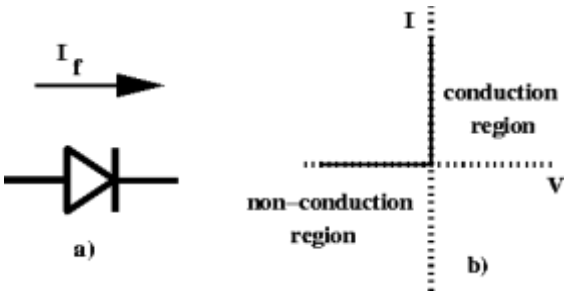


Figure a)Schematic symbol for a diode and b) current versus voltage for an ideal diode

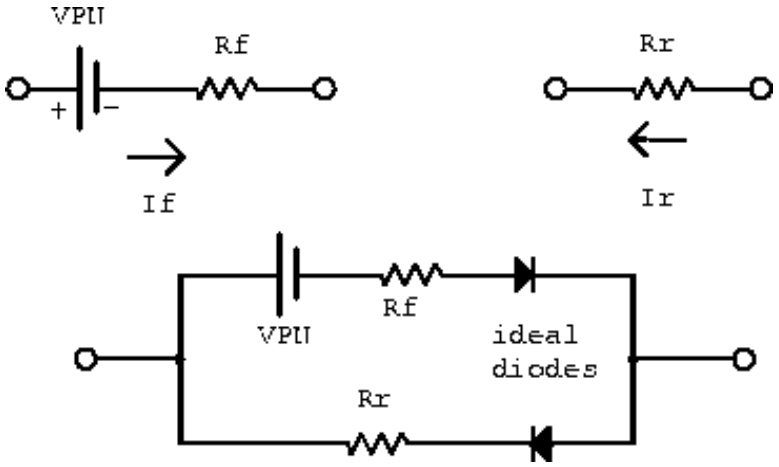


Figure 5.2 Equivalent circuit model of a junction diode

A diode can more accurately be described using the equivalent circuit model shown in figure 5.2. If a diode is forward biased with a high voltage it acts like a resistor (R_f) in series with a voltage source (V_{PN}). For reverse biasing it acts simply as a resistor (R_r). These approximations are referred to as the linear element model of a diode.

HALF-WAVE RECTIFIERS

Figure 5.3 shows a **half-wave rectifier** circuit. The voltage source V_S is an AC source

$$v_S(t) = V_m \sin(\omega t) \quad \text{……..(5.1)}$$

of frequency ω radians per second, and V_m is the maximum or peak voltage. Note that $\omega = 2\pi f$

where f is the frequency in Hz. Generally, the source v_S is the secondary winding of a transformer.

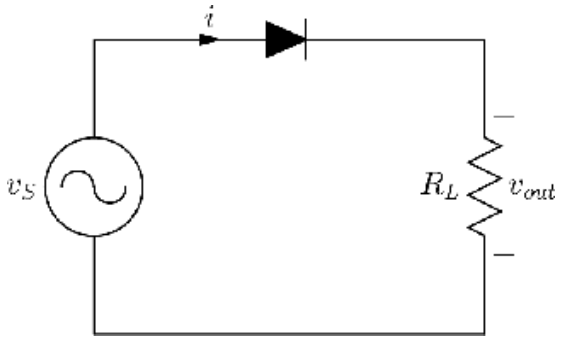


Figure 5.3 Half-wave rectifier

The diode is the component which does the rectification, since it permits current flow in one direction only. The resistor R_L represents the resistance of the load drawing the power.

Let's analyse this circuit assuming the diode is ideal. When $v_S > 0$, the diode is forward biased, and so switched on; therefore $v_{out} = v_S$. But when $v_S < 0$, the diode is reverse biased, i.e. switched off, and hence $v_{out} = 0$ V. This is illustrated in Figure 5.4.

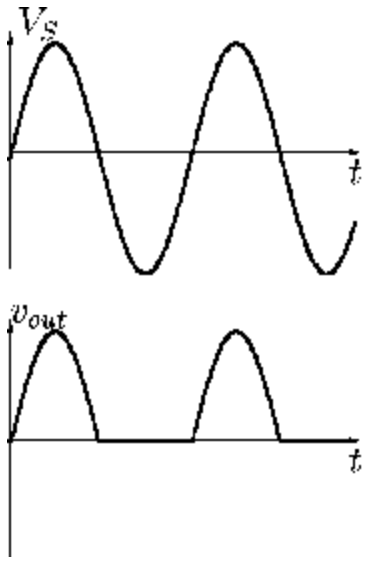


Figure 5.4 Half-wave rectifier waveforms

The load voltage waveform v_{out} is always positive, and so has a non-zero DC component, the average value V_{AVG} which we calculate as follows:

$$V_{AVG} = \frac{1}{T}\int_0^{T/2} V_m \sin(\omega t)\,dt$$

$$= \frac{V_m}{\pi}. \qquad \ldots\ldots(5.2)$$

If we use the practical diode model to take into account the diode voltage drop, then we need to reduce V_m by 0.7 V when forward biased:

$$V_{m(out)} = V_m - 0.7\ V \ldots\ldots(5.3)$$

and the average voltage becomes

$$V_{AVG} = \frac{V_{m(out)}}{\pi}. \qquad \ldots..(5.4)$$

This means that the average voltage is reduced by the forward bias voltage drop across the diode.

The **peak inverse voltage** (PIV) is defined as the peak voltage across the diode when reverse biased: (note that with zero current the voltage drop across R_L is zero)

$$PIV = V_m \ldots\ldots\ldots(5.5)$$

The diode must be capable of withstanding this voltage.

5.1.2 FULL-WAVE RECTIFIERS

In the half-wave rectifier the voltage is zero for half of the cycle. **Full-wave rectifiers** are designed using two or more diodes so that voltage is produced over the whole cycle.

Figure 5.5 shows a full-wave rectifier designed using two diodes and a center-tapped AC supply (i.e. center-tapped transformer).

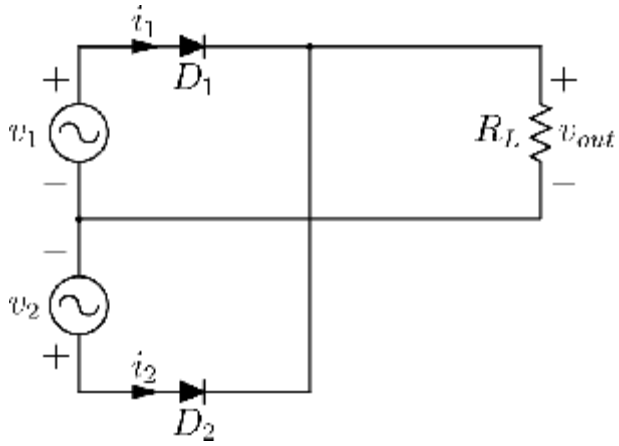


Figure 5.5 Center-tapped full-wave rectifier.

The waveforms are shown in Figure 5.6. The center tapping implies that the two source voltages v_1 and v_2 are a half cycle out of phase. We see that diode D_1 conducts when source v_1 is positive, and D_2 conducts when v_2 is positive, giving the waveform v_{out}.

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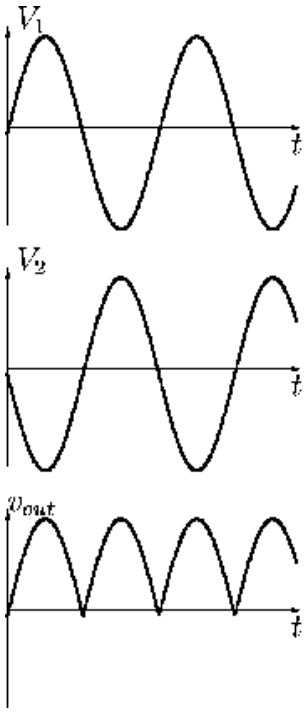


Figure 5.6 Full-wave rectifier waveforms

The average or DC value of the waveform v_{out} is now

$$V_{AVE} = \frac{2V_{m(out)}}{\pi} \quad \text{……..(5.6)}$$

since the waveform is non-zero twice as much as in the half-wave case. Here, $V_{m(out)}$ equals V_m if we regard the diodes as ideal, and equal to V_m -0.7 V if we use the practical model.

The peak inverse voltage is $PIV = 2V_m - 0.7\ V$ …..(5.7)

5.1.3 BRIDGE RECTIFIER

Figure shows a **bridge rectifier** built from four diodes and a single AC source. The waveform of v_{out} is the same as for the center-tapped full-wave rectifier.

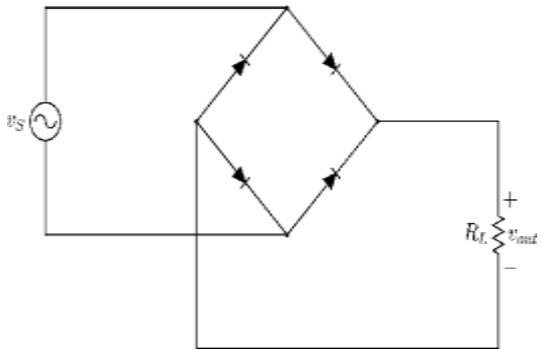


Figure 5.7 Bridge full-wave rectifier

The average voltage for the bridge rectifier is the same as in HWR but the peak inverse voltage is

$$PIV = V_m - 0.7\ V \quad \text{.....(5.8)}$$

5.1.4 CAPACITOR FILTERS

It can be seen from Figures that the waveform v_{out} is not very smooth. For many applications it is desired to have a much smoother DC waveform, and so a filtering circuit is used. We will consider the filtered half-wave rectifier of Figure, and leave the filtered full-wave rectifiers up to you to work out (not hard-see lab).

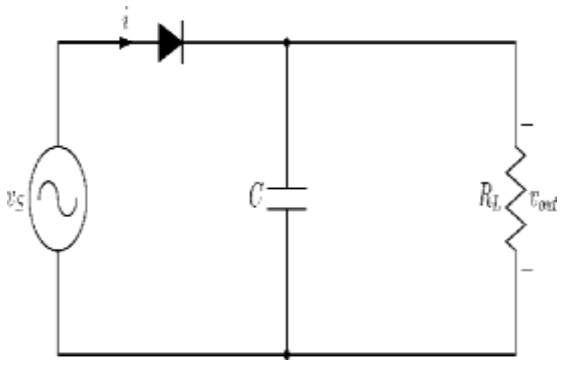


Figure 5.7 Filtered Half-wave rectifier.

The waveform produced by this filtered half-wave rectifier is shown in figure 5.8 illustrating the *ripple*.

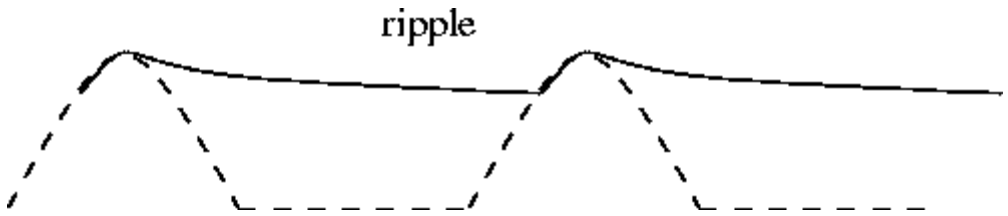


Figure 5.8 Ripple filtered Half-wave rectified waveform.

Here, ripple is defined as the difference between the maximum and minimum voltages on the waveform, Figure (i.e. peak-to-peak).

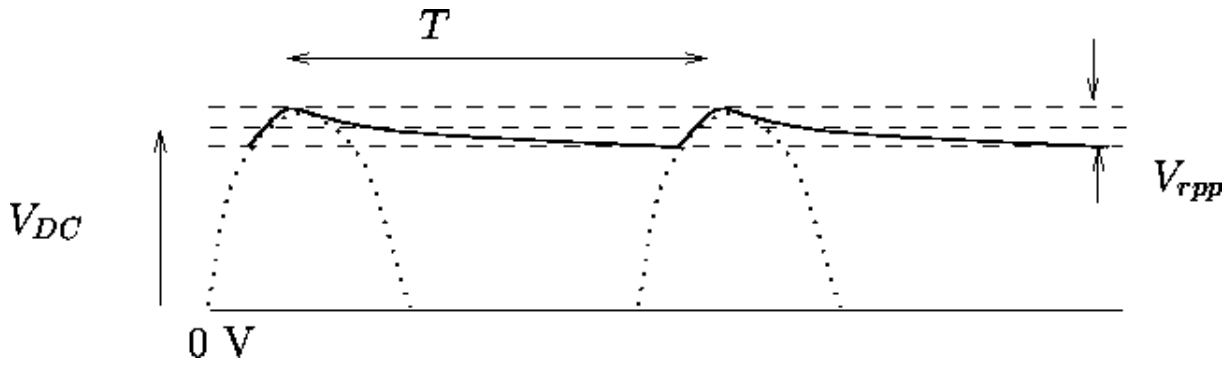


Figure 5.8 Filtered Half-wave rectified waveform showing V_{rpp} and V_{DC}.

The (peak-to-peak) **ripple factor** r is defined as

$$r = \frac{V_{rpp}}{V_{DC}} \quad \text{.....(5.9)}$$

where V_{rpp} is the peak-to-peak ripple voltage and V_{DC} is the DC component of the ripple waveform. T is the period of the AC source voltage: $T=1/f$, $\omega = 2\pi f$. For f=50 Hz (the frequency of the AC supply in Australia), T= 20 ms.

We now explain how to calculate (approximately) V_{rpp} and V_{DC}. Think of the ripple waveform as being approximated by a triangular waveform so that

$$V_{DC} = V_{m(out)} - \frac{V_{rpp}}{2} \quad \text{.....(5.10)}$$

Using symmetry. Suppose that at the beginning of a cycle the capacitor is fully charged to $V_{m(out)}$, and that the capacitor is large enough so that the time constant $R_L C$ is much larger than T. The rate of change of v_{out} at the beginning of the cycle t=0 is

$$-\frac{V_{m(out)}}{R_L C} \quad \text{.....(5.11)}$$

so that at time $t=T$ the capacitor voltage has decreased by an amount

$$V_{rpp} = \frac{V_{m(out)} T}{R_L C} \quad \text{.....(5.12)}$$

approximately (straight line approximation). This allows one to design C for a given load and desired ripple.

Exercise. Show that V_{rpp} in the case of a full-wave rectifier is given by

$$V_{rpp} = \frac{V_{m(out)} T}{2 R_L C}. \quad \text{.....(5.13)}$$

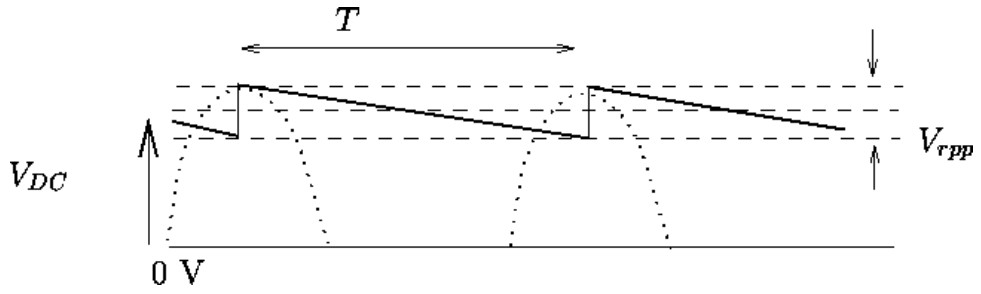


Figure 5.9 Approximate (triangular) filtered Half-wave rectified waveform

5.2 VOLTAGE REGULATORS:

The function of a voltage regulator is to provide a stable dc voltage for powering other electronic circuits. A voltage regulator should be capable of providing substantial output current. Voltage regulators are classified as:

- Series regulator
- Switching regulator

Series regulators use power transistor connected in series between the unregulated dc input and the load. The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor. Since the transistor conducts in the active or linear region, these regulators are also called linear regulators. Linear regulators may be fixed or variable output voltage and could be positive or negative. The schematic, important characteristics, data sheet, short circuit protection, current fold-back, current boosting techniques for linear voltage regulators such as 78 XX series, 723 IC are discussed.

Switching regulators, on the hand, operate the power transistor as a high frequency ***on/off*** switch, so that the power transistor does not conduct current continuously. This gives improved efficiency over series regulator.

5.2.1 SERIES OP-AMP REGULATOR

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations.

The above circuit shows a regulated supply.

- The circuit consists of the following four parts:
    1. Reference voltage circuit
    2. Error amplifier
    3. Series pass transistor

4. Feedback network

- The power transistor Q1 is in series with unregulated dc voltage Vin and regulated output voltage Vo.
- Whenever any fluctuation in the output voltage occurs, it must absorb the difference between the two voltages.
- The transistor Q1 is also connected as an emitter follower and therefore provides the sufficient current gain to drive the load.
- The output voltage is sampled by the R1-R2 divider and feedback to the negative input terminal of the op-amp error amplifier.
- This sampled voltage is compared with the reference voltage Vref.
- The output Vo of the error amplifier drives the series transistor Q1.
- Due to the variation in load current, if output voltage increases, the sampled voltage βVo increases.

$$\boxed{\beta = R2 / (R1+R2)} \quad \ldots\ldots(5.14)$$

- This reduces the output voltage Vo of the difference amplifier due to the 180' phase difference provided by the amplifier.
- Vo is applied to the base Q1 which is used as an emitter follower.
- Vo follows Vo' i.e. Vo also reduces.
- Hence the increase in Vo is nullified.
- Similarly reduction in output voltage also gets regulated.

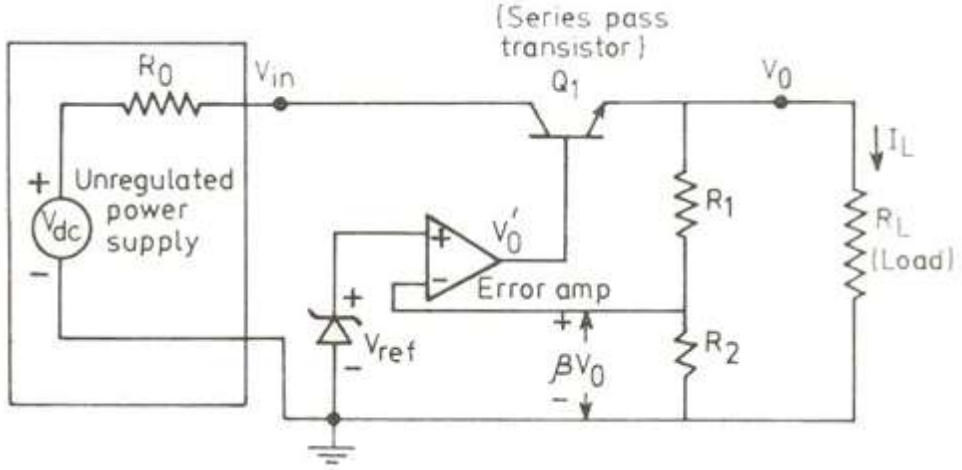


Figure 5.9 voltage regulator

Advantages:

1. Low cost
2. High reliability
3. Reduction in size
4. Excellent performance

Fixed voltage regulators : 78XX / 79XX series.

Adjustable voltage regulators : 723 Regulator.

5.2.2 IC REGULATOR

5.2.2.1 FIXED VOLTAGE REGULATOR

(1) **POSITIVE FIXED VOLTAGE REGULATORS**.

- 78XX series are three terminal, positive fixed regulators.In 78XX, the last two numbers 'XX' indicate the output voltage.There are seven output voltage options available such as 5, 6, 8,12,15,18 and 24V.For example 7805 represents 5V regulator.

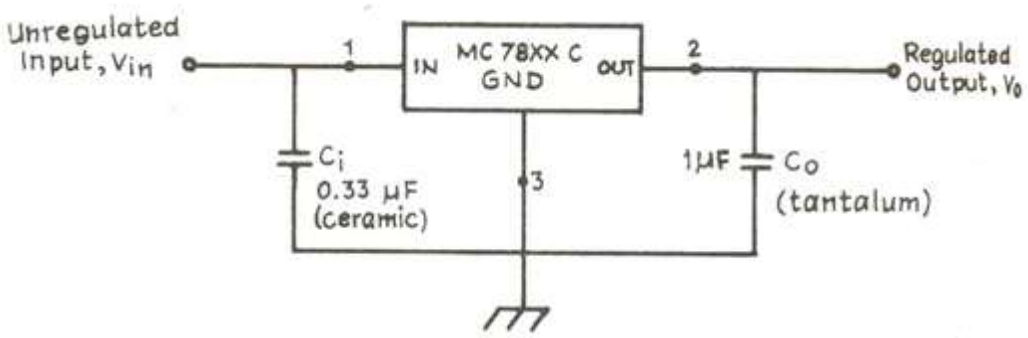


Figure 5.9 Positive fixed regulators

The above figure 5.9 shows the standard representation of monolithic 5 voltage regulator. A capacitor C_{in} (0.33 µF) is usually connected between the input terminal and ground to cancel the inductive effect due to long distribution leads. The output capacitor C_o (1 µF) improves the transmit response.

Characteristics:

- The regulated output voltage is fixed at a value specified by the manufacturer. For e.g. 78XX series has a output voltage at 5, 6, 8 etc.,
- The unregulated input voltage must be at least 2V more than the regulated output voltage i.e. | Vin | >= Vo +2 volts. For example, if 7805 regulator has Vo = 5V then Vin = 7V
- The load current Io_{max} may vary from 0 to rated maximum output current.
- Thermal shunt down : the IC has a temperature sensor (built-in) which turns off IC when it becomes too hot. The output current will drop and remain there until the IC has cooled significantly.

(2)Negative fixed voltage regulator:

- 79XX series of fixed output are negative voltage regulators.
- They are complement to the 78XX series.

- In addition to voltage options available in 78XX series, there are two extra voltage options of -2V and -5.2V available in 79XX series.
- The constructional detail is as same that of 78XX series.
- For example 7905 represents 5V regulator.

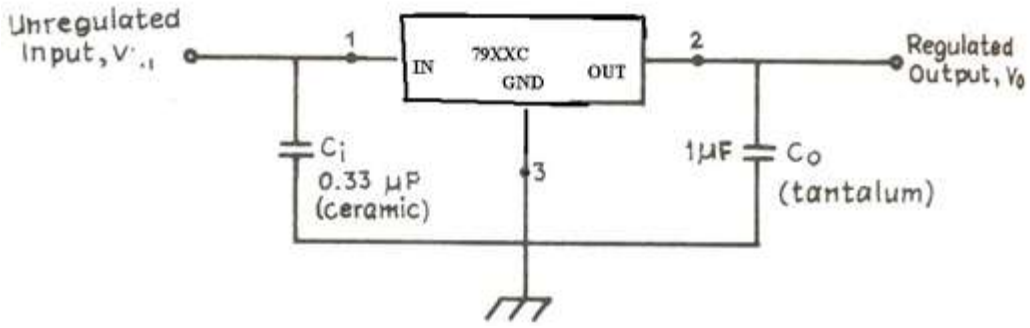


Figure 5.10 Negative fixed voltage regulator

5.2.3 VARIABLE VOLTAGE REGULATOR

The three terminal regulators discussed earlier have the following limitations

1.No short circuit operation

2. Output voltage is fixed.

These limitations have been overcome in the 723 general purpose regulator, which can be adjusted over a wide range of both positive or negative regulated voltage. This IC is inherently low current device, but can be boosted to provide 5 amps or more current by connecting external components.

Limitation:

It also has no short circuit current limits.

It has no in-built thermal protection.

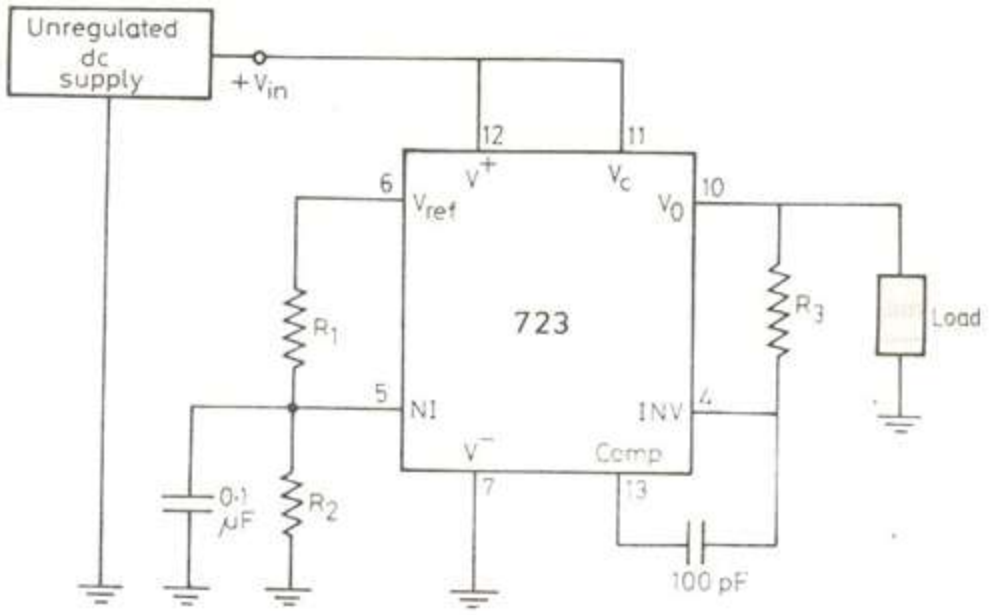
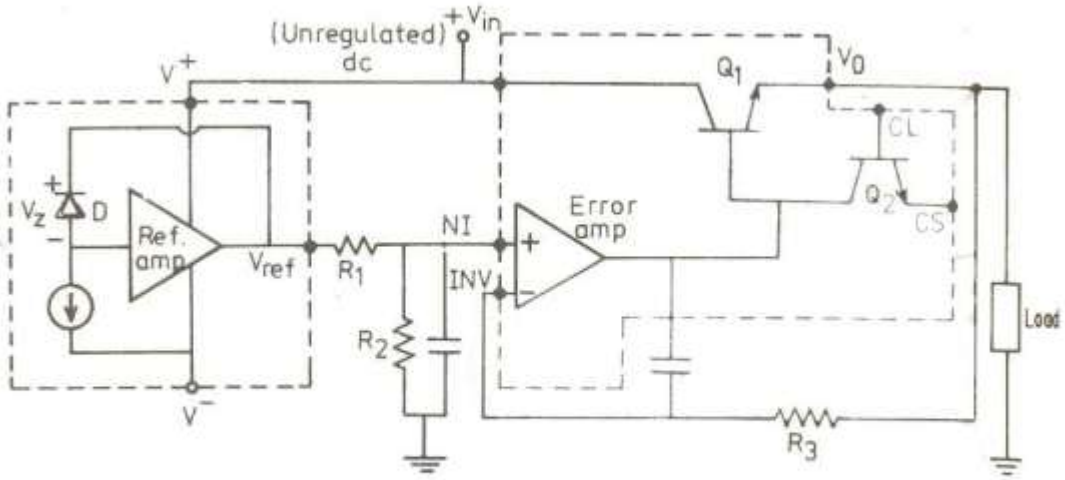


Figure 5.11 723 general purpose regulator



Functional diagram for a low voltage regulator

$V_{ref} \simeq 7V$, $V_o = V_{NI} = 7R_2/(R_1 + R_2)$, $V^+ = +V_{cc}$, $R_3 = R_1 \parallel R_2$ (minimum drift), $V^- = \text{Gnd}$.

Figure 5.12 Low voltage regulator

5.2.4 BOOSTING OUTPUT CURRENT FOR FIXED IC REGULATOR:

- It is possible to boost the output current of a three terminal regulator by connecting an external pass transistor in parallel with the regulator.
- For low load currents, the voltage drop across R1 is insufficient (<0.7 V) to turn on transistor Q1 and the regulator itself is able to supply the load current.
- As I_L increases, the voltage drop across R1 increases.
- When the voltages drop is ~ 0.7 V, the transistor Q1 turns on.
- For example if I_L = 100 mA;

Voltage drop across R1 = 7 Ω * 100 mA

= 0.7 mA.

- Thus if I_L increases more than 100 mA, the transistor Q1 turns on and supplies the constant extra current required.
- Since Veb (ON) remains fairly constant, the excess current comes from Q1 and base after amplification by β.

The regulator adjusts I_B so that $I_L=I_C+I_0$

$I_C=\beta I_B$

For the regulator

$I_o=I_i-I_q$

$I_O = I_i - I_Q$

$\approx I_i$ **(as I_Q is small)**

$I_B = I_i - I_{R1}$

$\approx I_O - \frac{V_{EB(on)}}{R_1}$

The maximum current Io(max) for a 7805 regulator is 1A from the data, assuming Veb(on)= 1 V& β = 15 we get from equation (8),

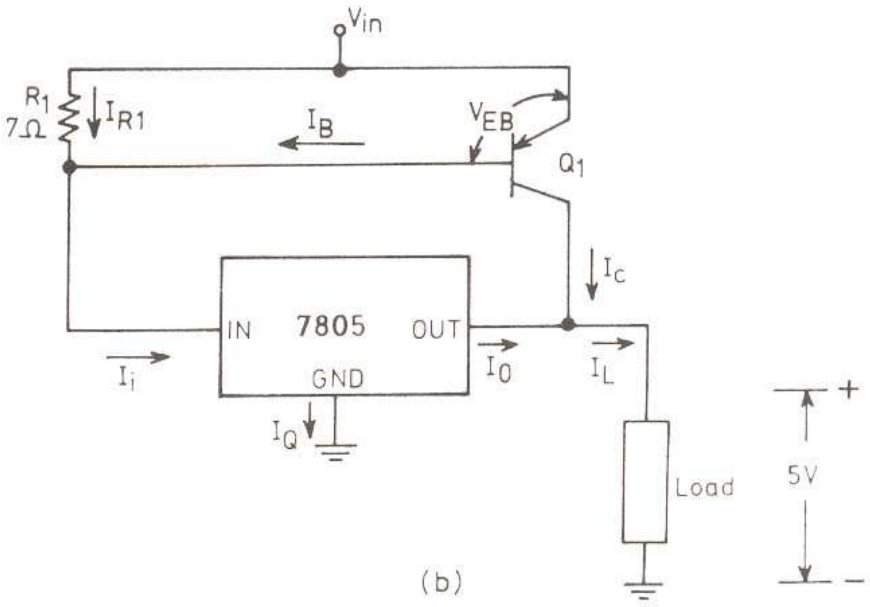


Figure 5.13 Fixed voltage regulator

5.2.4 VARIABLE VOLTAGE REGULATOR

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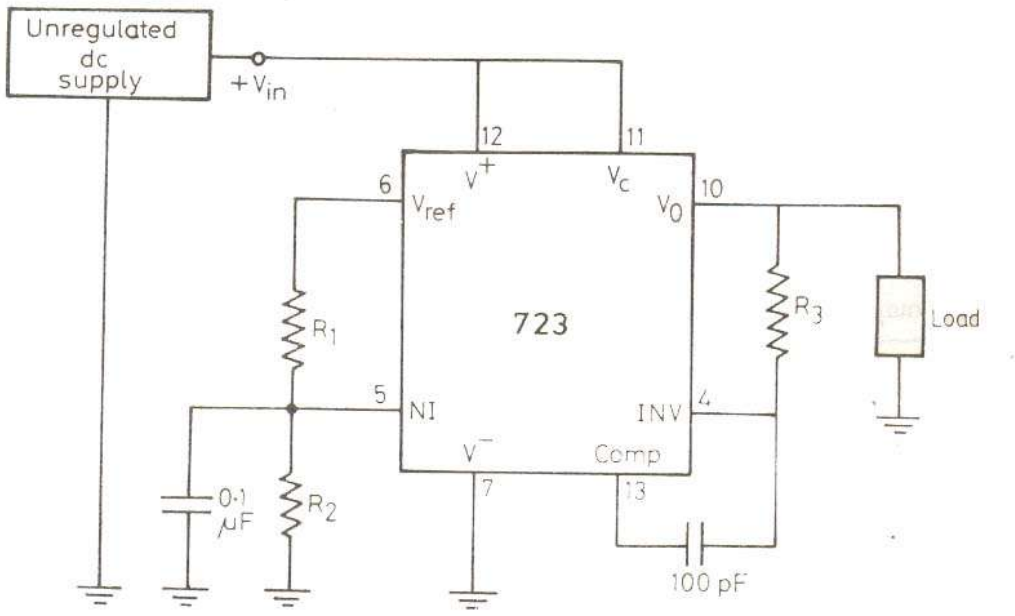
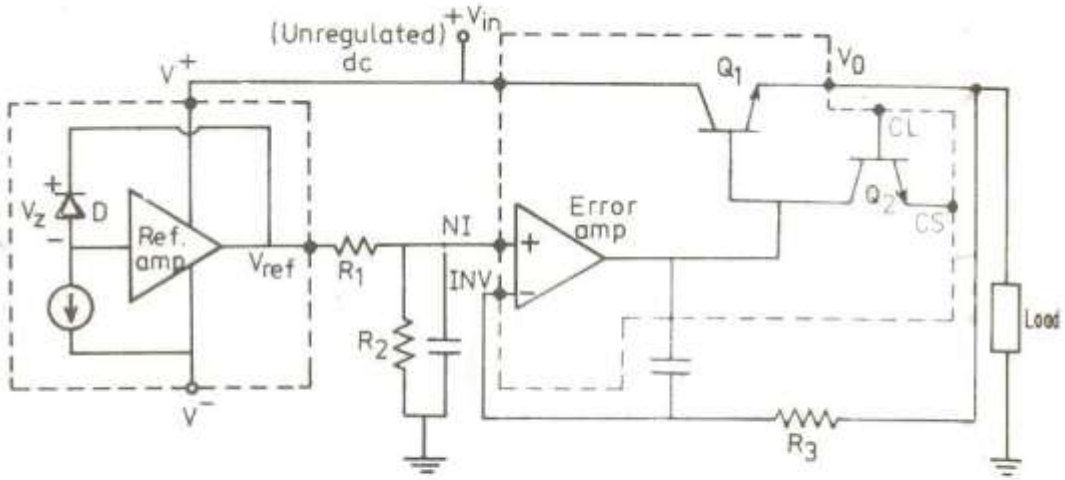
LIMITATION:

- It also has no short circuit current limits.
- It has no in-built thermal protection.



A low voltage regulator using 723 IC

Figure 5.12 723 IC Low voltage regulator



Functional diagram for a low voltage regulator

$V_{ref} \simeq 7V$, $V_o = V_{NI} = 7R_2/(R_1 + R_2)$, $V^+ = +V_{cc}$, $R_3 = R_1 \parallel R_2$ (minimum drift), $V^- = \text{Gnd}$.

Figure 5.12 Functional block for a Low voltage regulator

Photodiode Characteristics and Applications

Silicon photodiodes are semiconductor devices responsive to high-energy particles and photons. Photodiodes operate by absorption of photons or charged particles and generate a flow of current in an external circuit, proportional to the incident power.

Photodiodes can be used to detect the presence or absence of minute quantities of light and can be calibrated for extremely accurate measurements from intensities below 1 pW/cm² to intensities above 100 mW/cm².

Silicon photodiodes are utilized in such diverse applications as :

- Spectroscopy
- Photography
- Analytical instrumentation
- Optical position sensors
- Beam alignment
- Surface characterization
- Laser range finders
- Optical communications
- Medical imaging instruments

PLANAR DIFFUSED SILICON PHOTODIODE CONSTRUCTION

Planar diffused silicon photodiodes are simply P-N junction diodes. A P-N junction can be formed by diffusing either a P-type impurity (anode), such as Boron, into a N-type bulk silicon wafer, or a N-type impurity, such as Phosphorous, into a P-type bulk silicon wafer. The diffused area defines the photodiode active area. To form an ohmic contact another impurity diffusion into the backside of the wafer is necessary. The impurity is an N-type for P-type active area and P-type for an N-type active area. The contact pads are deposited on the front active area on defined areas, and on the backside, completely covering the device. The active area is then passivated with an anti-reflection coating to reduce the reflection of the light for a specific predefined wavelength. The non-active area on the top is covered with a thick layer of silicon oxide. By controlling the thickness of bulk substrate, the speed and responsivity of the photodiode can be controlled. Note that the photodiodes, when biased, must be operated in the reverse bias mode, i.e. a negative voltage applied to anode and positive voltage to cathode.

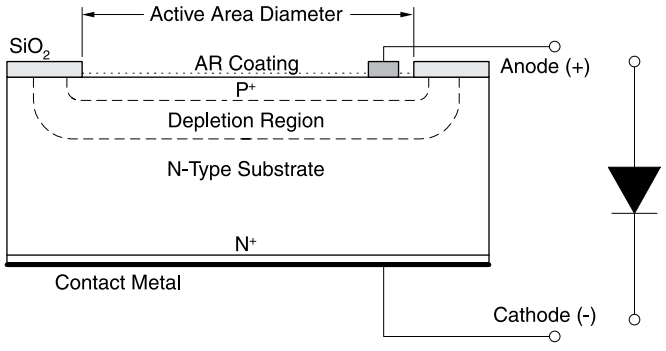


Figure 1. Planar diffused silicon photodiode

PRINCIPLE OF OPERATION

Silicon is a semiconductor with a band gap energy of 1.12 eV at room temperature. This is the gap between the valence band and the conduction band. At absolute zero temperature the valence band is completely filled and the conduction band is vacant. As the temperature increases, the electrons become excited and escalate from the valence band to the conduction band by thermal energy. The electrons can also be escalated to the conduction band by particles or photons with energies greater than 1.12eV, which corresponds to wavelengths shorter than 1100 nm. The resulting electrons in the conduction band are free to conduct current.

Due to concentration gradient, the diffusion of electrons from the N-type region to the P-type region and the diffusion of holes from the P-type region to the N-type region, develops a built-in voltage across the junction. The inter-diffusion of electrons and holes between the N and P regions across the junction results in a region with no free carriers. This is the depletion region. The built-in voltage across the depletion region results in an electric field with maximum at the junction and no field outside of the depletion region. Any applied reverse bias adds to the built in voltage and results in a wider depletion region. The electron-hole pairs generated by light are swept away by drift in the depletion region and are collected by diffusion from the undepleted region. The current generated is proportional to the incident light or radiation power. The light is absorbed exponentially with distance and is proportional to the absorption coefficient. The absorption coefficient is very high for shorter wavelengths in the UV region and is small for longer wavelengths (Figure 2). Hence, short wavelength photons such as UV, are absorbed in a thin top surface layer while silicon becomes transparent to light wavelengths longer than 1200 nm. Moreover, photons with energies smaller than the band gap are not absorbed at all.

(continued)

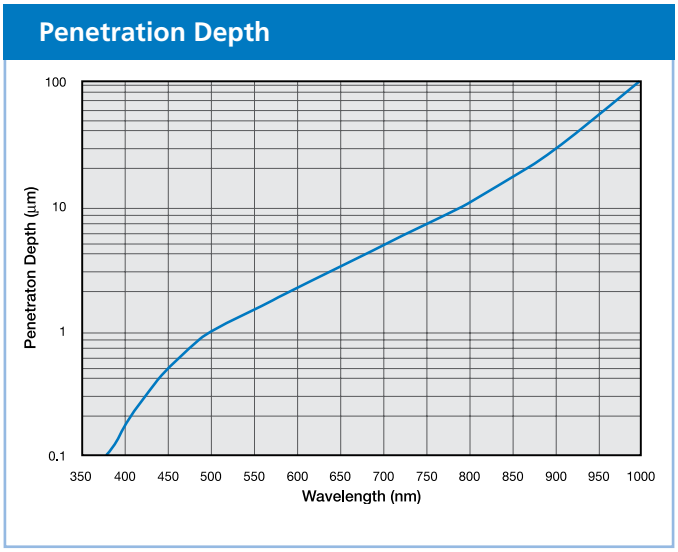


Figure 2. Penetration depth (1/e) of light into silicon substrate for various wavelengths.

ELECTRICAL CHARACTERISTICS

A silicon photodiode can be represented by a current source in parallel with an ideal diode (Figure. 3). The current source represents the current generated by the incident radiation, and the diode represents the p-n junction. In addition, a ***junction capacitance*** (C_j) and a ***shunt resistance*** (R_{SH}) are in parallel with the other components. ***Series resistance*** (R_S) is connected in series with all components in this model.

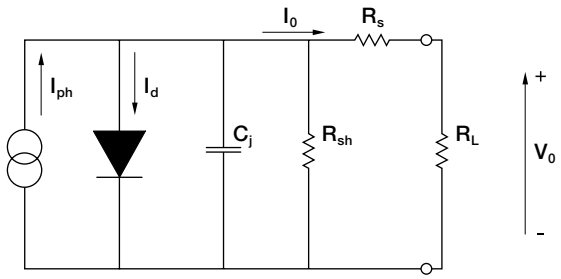


Figure 3. Equivalent Circuit for the silicon photodiode

Shunt Resistance, R_{SH}

Shunt resistance is the slope of the current-voltage curve of the photodiode at the origin, i.e. V=0. Although an ideal photodiode should have an infinite shunt resistance, actual values range from 10's to 1000's of Mega ohms. Experimentally it is obtained by applying ±10 mV, measuring the current and calculating the resistance. Shunt resistance is used to determine the noise current in the photodiode with no bias (photovoltaic mode). For best photodiode performance the highest shunt resistance is desired.

Series Resistance, R_S

Series resistance of a photodiode arises from the resistance of the contacts and the resistance of the undepleted silicon (Figure 1). It is given by:

$$R_S = \frac{(W_S - W_d)\rho}{A} + R_C \qquad (1)$$

Where W_S is the thickness of the substrate, W_d is the width of the depleted region, ***A*** is the diffused area of the junction, ρ is the resistivity of the substrate and R_C is the contact resistance. Series resistance is used to determine the linearity of the photodiode in photovoltaic mode (no bias, V=0). Although an ideal photodiode should have no series resistance, typical values ranging from 10 to 1000 Ω's are measured.

Junction Capacitance, C_J

The boundaries of the depletion region act as the plates of a parallel plate capacitor (Figure 1). The junction capacitance is directly proportional to the diffused area and inversely proportional to the width of the depletion region. In addition, higher resistivity substrates have lower junction capacitance. Furthermore, the capacitance is dependent on the reverse bias as follows:

$$C_J = \frac{\epsilon_{Si}\epsilon_0 A}{\sqrt{2\epsilon_{Si}\epsilon_0\mu\rho(V_A + V_{bi})}} \qquad (2)$$

$$= A\sqrt{\frac{\epsilon_{Si}\epsilon_0}{2\mu\rho(V_A + V_{bi})}}$$

$$= \frac{\epsilon_{Si}\epsilon_0 A}{W_d}$$

$$\text{Depletion Depth } W_d = \sqrt{2\epsilon_{Si}\epsilon_0\mu\rho(V_A + V_{bi})}$$

Typical Capacitance vs. Reverse Bias

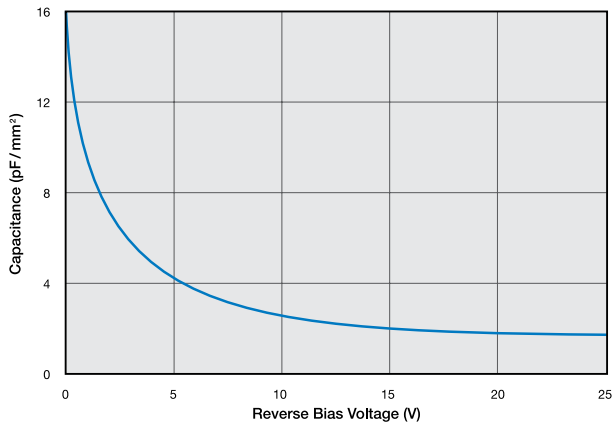


Figure 4. Capacitance of Photoconductive Devices versus Reverse Bias Voltage

where ϵ_0= 8.854x10^{-14} F/cm, is the permittivity of free space, ϵ_{Si}=11.9 is the silicon dielectric constant, μ = 1400 cm²/Vs is the mobility of the electrons at 300 K, ρ is the resistivity of the silicon, V_{bi} is the built-in voltage of silicon and V_A is the applied bias. Figure 4 shows the dependence of the capacitance on the applied reverse bias voltage. Junction capacitance is used to determine the speed of the response of the photodiode.

Rise / Fall Time and Frequency Response, t_r / t_f / f_{3dB}

The rise time and fall time of a photodiode is defined as the time for the signal to rise or fall from 10% to 90% or 90% to 10% of the final value respectively. This parameter can be also expressed as frequency response, which is the frequency at which the photodiode output decreases by 3dB. It is roughly approximated by:

$$t_r \cong \frac{0.35}{f_{3db}} \qquad (3)$$

There are three factors defining the response time of a photodiode:

1. t_{DRIFT}, the charge collection time of the carriers in the depleted region of the photodiode.

2. $t_{DIFFUSED}$, the charge collection time of the carriers in the undepleted region of the photodiode.

3. t_{RC}, the RC time constant of the diode-circuit combination.

t_{RC} is determined by t_{RC}=2.2 RC, where R, is the sum of the diode series resistance and the load resistance (R_S + R_L), and C, is the sum of the photodiode junction and the stray capacitances (C_j+C_s). Since the junction capacitance (C_j) is dependent on the diffused area of the photodiode and the applied reverse bias (Equation 2), faster rise times are obtained with smaller diffused area photodiodes, and larger applied reverse biases. In addition, stray capacitance can be minimized by using short leads, and careful lay-out of the electronic components. The total rise time is determined by:

$$t_R = \sqrt{t_{DRIFT}^{\,2} + t_{DIFFUSED}^{\,2} + t_{RC}^{\,2}} \qquad (4)$$

Generally, in photovoltaic mode of operation (no bias), rise time is dominated by the diffusion time for diffused areas less than 5 mm² and by RC time constant for larger diffused areas for all wavelengths. When operated in photoconductive mode (applied reverse bias), if the photodiode is fully depleted, such as high speed series, the dominant factor is the drift time. In non-fully depleted photodiodes, however, all three factors contribute to the response time.

OPTICAL CHARACTERISTICS

Responsivity, R $_\lambda$

The responsivity of a silicon photodiode is a measure of the sensitivity to light, and it is defined as the ratio of the photocurrent I_P to the incident light power P at a given wavelength:

$$R_\lambda = \frac{I_P}{P} \qquad (5)$$

In other words, it is a measure of the effectiveness of the conversion of the light power into electrical current. It varies with the wavelength of the incident light (Figure 5) as well as applied reverse bias and temperature.

Typical Spectral Response

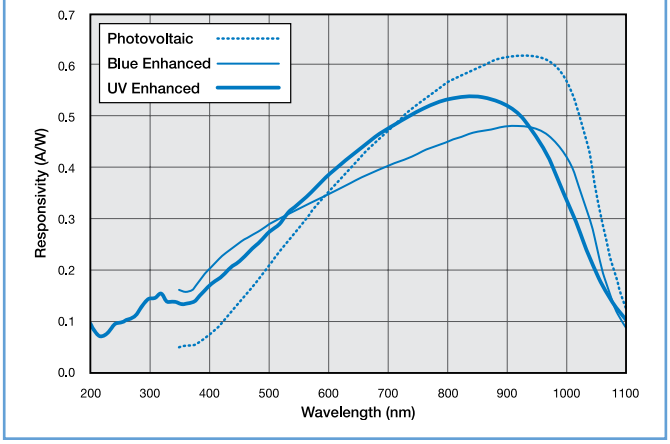


Figure 5. Typical Spectral Responsivity of Several Different Types of Planar Diffused Photodiodes

Responsivity increases slightly with applied reverse bias due to improved charge collection efficiency in the photodiode. Also there are responsivity variations due to change in temperature as shown in figure 6. This is due to decrease or increase of the band gap, because of increase or decrease in the temperature respectively. Spectral responsivity may vary from lot to lot and it is dependent on wavelength. However, the relative variations in responsivity can be reduced to less than 1% on a selected basis.

Temperature Dependence of Responsivity

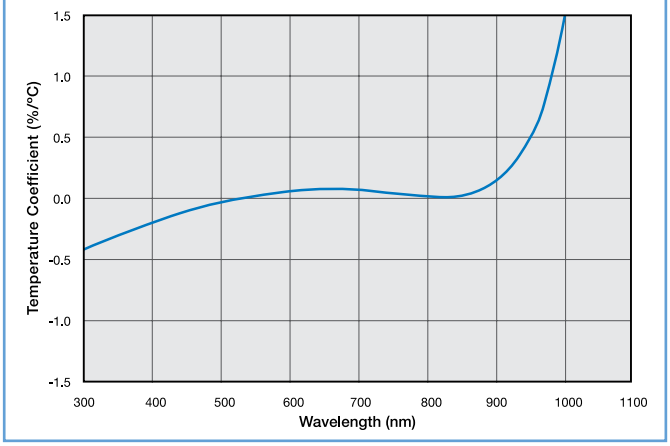


Figure 6. Typical Temperature Coefficient of Responsivity For Silicon Photodiode

Quantum Efficiency, Q.E.

Quantum efficiency is defined as the fraction of the incident photons that contribute to photocurrent. It is related to responsivity by:

$$Q.E. = \frac{R_{\lambda\ Observed}}{R_{\lambda\ Ideal}} \qquad (6)$$

$$= R_\lambda \frac{hc}{\lambda q}$$

$$= 1240 \frac{R_\lambda}{\lambda}$$

where h=6.63 x 10^{-34} J-s, is the Planck constant, c=3 x 10^{8} m/s, is the speed of light, q=1.6 x 10^{-19} C, is the electron charge, R_λ is the responsivity in A/W and λ is the wavelength in nm.

Non-Uniformity

Non-Uniformity of response is defined as variations of responsivity observed over the surface of the photodiode active area with a small spot of light. Non-uniformity is inversely proportional to spot size, i.e. larger non-uniformity for smaller spot size.

Non-Linearity

A silicon photodiode is considered linear if the generated photocurrent increases linearly with the incident light power. Photocurrent linearity is determined by measuring the small change in photocurrent as a result of a small change in the incident light power as a function of total photocurrent or incident light power. Non-Linearity is the variation of the ratio of the change in photocurrent to the same change in light power, i.e. $\Delta I/\Delta P$. In another words, linearity exhibits the consistency of responsivity over a range of light power. Non-linearity of less than ±1% are specified over 6-9 decades for planar diffused photodiodes. The lower limit of the photocurrent linearity is determined by the noise current and the upper limit by the series resistance and the load resistance. As the photocurrent increases, first the non-linearity sets in, gradually increasing with increasing photocurrent, and finally at saturation level, the photocurrent remains constant with increasing incident light power. In general, the change in photocurrent generated for the same change in incident light power, is smaller at higher current levels, when the photodetector exhibits non-linearity. The linearity range can slightly be extended by applying a reverse bias to the photodiode.

(continued)

I-V CHARACTERISTICS

The current-voltage characteristic of a photodiode with no incident light is similar to a rectifying diode. When the photodiode is forward biased, there is an exponential increase in the current. When a reverse bias is applied, a small reverse saturation current appears. It is related to dark current as:

$$I_D = I_{SAT}\left(e^{\frac{qV_A}{k_BT}} - 1\right) \quad (7)$$

where I_D is the photodiode dark current, I_{SAT} is the reverse saturation current, q is the electron charge, V_A is the applied bias voltage, k_B=1.38 x 10^{-23} J / K, is the Boltzmann Constant and T is the absolute temperature (273 K= 0 °C).

Photodetector I-V Curves

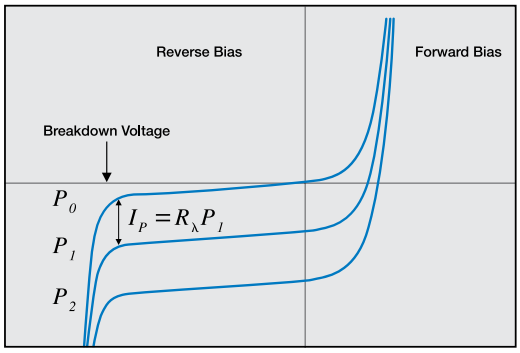


Figure 7. Characteristic I-V Curves of an OSI Optoelectronics photodiode for Photoconductive and Photovoltaic modes of operation. P_0-P_2 represent different light levels.

This relationship is shown in figure 7. From equation 7, three various states can be defined:

a) V = 0, In this state, the dark current I_P=0.
b) V = +V, In this state the current increases exponentially. This state is also known as forward bias mode.
c) V = -V, When a very large reverse bias is applied to the photodiode, the dark current becomes the reverse saturation current, I_{Sat}.

Illuminating the photodiode with optical radiation, shifts the I-V curve by the amount of photocurrent (I_P). Thus:

$$I_{TOTAL} = I_{SAT}\left(e^{\frac{qV_A}{k_BT}} - 1\right) - I_P \quad (8)$$

where I_P is defined as the photocurrent in equation 5.

As the applied reverse bias increases, there is a sharp increase in the photodiode current. The applied reverse bias at this point is referred to as breakdown voltage. This is the maximum applied reverse bias, below which, the photodiode should be operated (also known as maximum reverse voltage). Breakdown voltage, varies from one photodiode to another and is usually measured, for small active areas, at a dark current of 10 µA.

NOISE

In a photodiode, two sources of noise can be identified; Shot noise and Johnson noise:

Shot Noise

Shot noise is related to the statistical fluctuation in both the photocurrent and the dark current. The magnitude of the shot noise is expressed as the root mean square (rms) noise current:

$$I_{sn} = \sqrt{2q(I_P + I_D)\Delta f} \quad (9)$$

Where q=1.6x10^{-19}C, is the electron charge, I_P is the photogenerated current, I_D is the photodetector dark current and Δf is the noise measurement bandwidth. Shot noise is the dominating source when operating in photoconductive (biased) mode.

Thermal or Johnson Noise

The shunt resistance in a photodetector has a Johnson noise associated with it. This is due to the thermal generation of carriers. The magnitude of this generated noise current is:

$$I_{jn} = \sqrt{\frac{4k_B T\Delta f}{R_{SH}}} \quad (10)$$

Where k_B=1.38 x 10^{-23} J/K, is the Boltzmann Constant, T, is the absolute temperature in degrees Kelvin (273 K= 0 °C), Δf is the noise measurement bandwidth and R_{SH} , is the shunt resistance of the photodiode. This type of noise is the dominant current noise in photovoltaic (unbiased) operation mode.

Note: All resistors have a Johnson noise associated with them, including the load resistor. This additional noise current is large and adds to the Johnson noise current caused by the photodetector shunt resistance.

Total Noise

The total noise current generated in a photodetector is determined by:

$$I_{tn} = \sqrt{I_{sn}^{\,2} + I_{jn}^{\,2}} \quad (11)$$

Noise Equivalent Power (NEP)

Noise Equivalent Power is the amount of incident light power on a photodetector, which generates a photocurrent equal to the noise current. NEP is defined as:

$$NEP = \frac{I_{tn}}{R_\lambda} \quad (12)$$

Where R_λ is the responsivity in A/W and I_{tn} is the total noise of the photodetector. NEP values can vary from 10^{-11} W/√Hz for large active area photodiodes down to 10^{-15} W /√Hz for small active area photodiodes.

(continued)

TEMPERATURE EFFECTS

All photodiode characteristics are affected by changes in temperature. They include shunt resistance, dark current, breakdown voltage, responsivity and to a lesser extent other parameters such as junction capacitance.

Shunt Resistance and Dark Current:

There are two major currents in a photodiode contributing to dark current and shunt resistance. Diffusion current is the dominating factor in a photovoltaic (unbiased) mode of operation, which determines the shunt resistance. It varies as the square of the temperature. In photoconductive mode (reverse biased), however, the drift current becomes the dominant current (dark current) and varies directly with temperature. Thus, change in temperature affects the photodetector more in photovoltaic mode than in photoconductive mode of operation.

In photoconductive mode the dark current may approximately double for every 10 °C increase change in temperature. And in photovoltaic mode, shunt resistance may approximately double for every 6 °C decrease in temperature. The exact change is dependent on additional parameters such as the applied reverse bias, resistivity of the substrate as well as the thickness of the substrate.

Breakdown Voltage:

For small active area devices, by definition breakdown voltage is defined as the voltage at which the dark current becomes 10μA. Since dark current increases with temperature, therefore, breakdown voltage decreases similarly with increase in temperature.

Responsivity:

Effects of temperature on responsivity is discussed in the “Responsivity” section of these notes.

BIASING

A photodiode signal can be measured as a voltage or a current. Current measurement demonstrates far better linearity, offset, and bandwidth performance. The generated photocurrent is proportional to the incident light power and it must be converted to voltage using a transimpedance configuration. The photodiode can be operated with or without an applied reverse bias depending on the application specific requirements. They are referred to as “Photoconductive” (biased) and “Photovoltaic” (unbiased) modes.

Photoconductive Mode (PC)

Application of a reverse bias (i.e. cathode positive, anode negative) can greatly improve the speed of response and linearity of the devices. This is due to increase in the depletion region width and consequently decrease in junction capacitance. Applying a reverse bias, however, will increase the dark and noise currents. An example of low light level / high-speed response operated in photoconductive mode is shown in figure 8.

In this configuration the detector is biased to reduce junction capacitance thus reducing noise and rise time (t_r). A two stage amplification is used in this example since a high gain with a wide bandwidth is required. The two stages include a transimpedance pre-amp for current- to-voltage conversion and a non-inverting amplifier for voltage amplification. Gain and bandwidth ($f_{3dB\ Max}$) are directly determined by R_F, per equations (13) and (14) . The gain of the second stage is approximated by 1+ R1 / R2. A feedback capacitor (C_F) will limit the frequency response and avoids gain peaking.

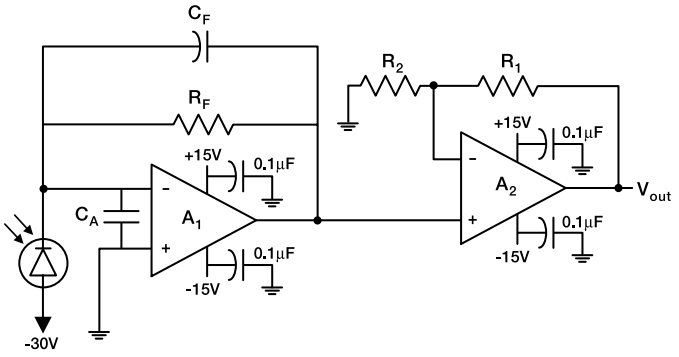


Figure 8. Photoconductive mode of operation circuit example: Low Light Level / Wide Bandwidth

$$f_{3dB\mathrm{Max}}[Hz] = \sqrt{\frac{GBP}{2\pi R_F (C_J + C_F + C_A)}} \qquad (13)$$

Where GBP is the Gain Bandwidth Product of amplifier (A_1) and C_A is the amplifier input capacitance.

$$Gain(V/W) = \frac{V_{OUT}}{P} = R_F\left(1 + \frac{R_1}{R_2}\right)R_\lambda \qquad (14)$$

In low speed applications, a large gain, e.g. >10MΩ can be achieved by introducing a large value (R_F) without the need for the second stage.

Typical components used in this configuration are:

Amplifier :	OPA-637, OPA-846, OPA-847, or similar
R_F:	1 to 10 KΩ Typical, depending on C_j
R_1:	10 to 50 kΩ
R_2:	0.5 to 10 kΩ
C_F:	0.2 to 2 pF

In high speed, high light level measurements, however, a different approach is preferred. The most common example is pulse width measurements of short pulse gas lasers, solid state laser diodes, or any other similar short pulse light source. The photodiode output can be either directly connected to an oscilloscope (Figure 9) or fed to a fast response amplifier. When using an oscilloscope, the bandwidth of the scope can be adjusted to the pulse width of the light source for maximum signal to noise ratio. In this application the bias voltage is large. Two opposing protection diodes should be connected to the input of the oscilloscope across the input and ground.

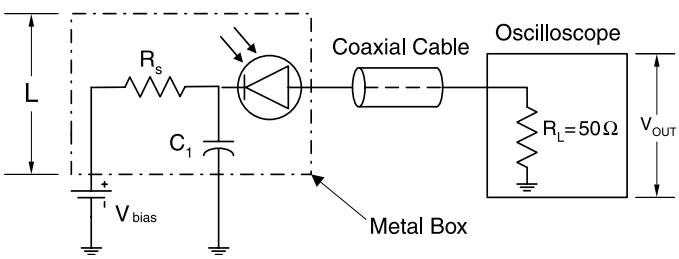


Figure 9. Photoconductive mode of operation circuit example: High Light Level / High Speed Response

(continued)

To avoid ringing in the output signal, the cable between the detector and the oscilloscope should be short (i.e. < 20cm) and terminated with a 50 ohm load resistor (R_L). The photodiode should be enclosed in a metallic box, if possible, with short leads between the detector and the capacitor, and between the detector and the coaxial cable. The metallic box should be tied through a capacitor (C1), with lead length (L) less than 2 cm, where R_L C_1 > 10 τ (τ is the pulse width in seconds). R_S is chosen such that R_S < V_{BIAS} / 10 I_{PDC}, where I_{PDC} is the DC photocurrent. Bandwidth is defined as 0.35 / τ. A minimum of 10V reverse bias is necessary for this application. Note that a bias larger than the photodiode maximum reverse voltage should not be applied.

Photovoltaic Mode (PV)

The photovoltaic mode of operation (unbiased) is preferred when a photodiode is used in low frequency applications (up to 350 kHz) as well as ultra low light level applications. In addition to offering a simple operational configuration, the photocurrents in this mode have less variations in responsivity with temperature. An example of an ultra low light level / low speed is shown in figure 10.

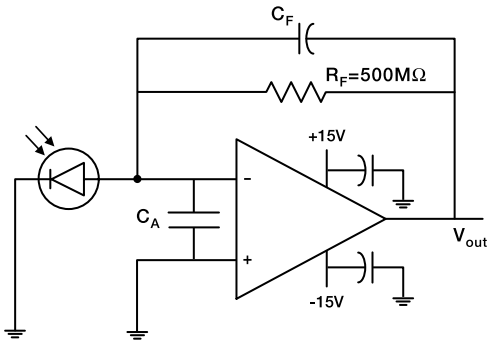


Figure 10. Photovoltaic mode of operation circuit example: Ultra low level light / low speed

In this example, a FET input operational amplifier as well as a large resistance feedback resistor (R_F) is considered. The detector is unbiased to eliminate any additional noise current. The total output is determined by equation (15) and the op-amp noise current is determined by R_F in equation (16):

$$V_{OUT} = I_P \times R_F \qquad (15)$$

$$I_N \left[\frac{A_{rms}}{\sqrt{Hz}}\right] = \sqrt{\frac{4kT}{R_F}} \qquad (16)$$

where k=1.38 x 10^{-23} J/K and T is temperature in K.

For stability, select C_F such that

$$\sqrt{\frac{GBP}{2\pi R_F (C_J + C_F + C_A)}} > \frac{1}{2\pi R_F C_F} \qquad (17)$$

Operating bandwidth, after gain peaking compensation is:

$$f_{OP}[Hz] = \frac{1}{2\pi R_F C_F} \qquad (18)$$

Some recommended components for this configuration are:

Amplifier :	OPA111, OPA124, OPA627 or similar
R_F :	500 MΩ

These examples or any other configurations for single photodiodes can be applied to any of OSI Optoelectronics' monolithic, common substrate liner array photodiodes. The output of the first stage pre-amplifiers can be connected to a sample and hold circuit and a multiplexer. Figure 11 shows the block diagram for such configuration.

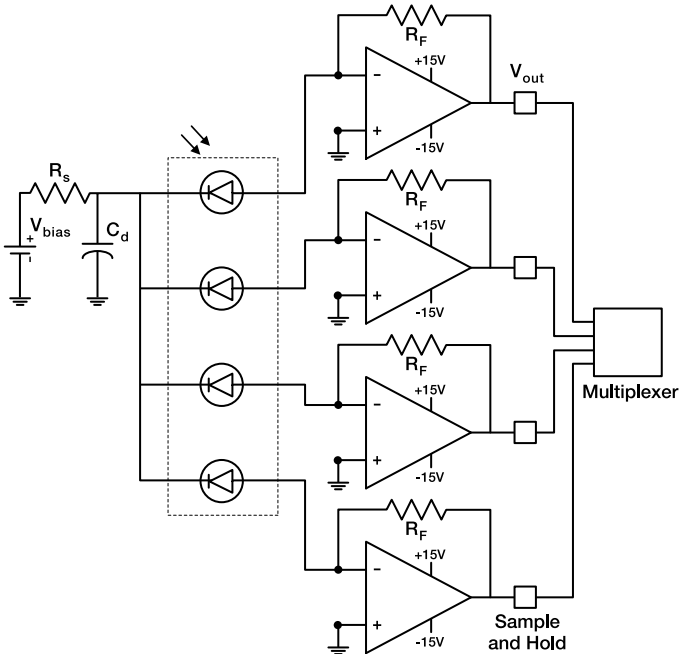
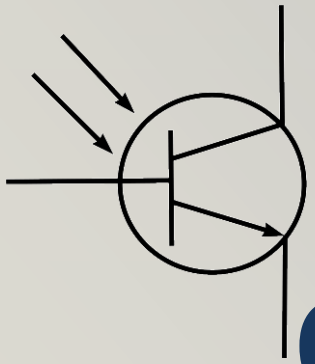
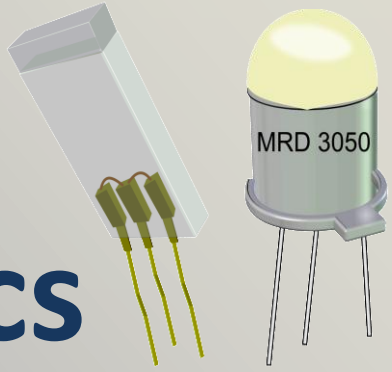


Figure 11. Circuit example for a multi-element, common cathode array



Lesson 1452, Optoelectronics



Experiment 6, Photodiode and Phototransistor Current Measurements

Objectives

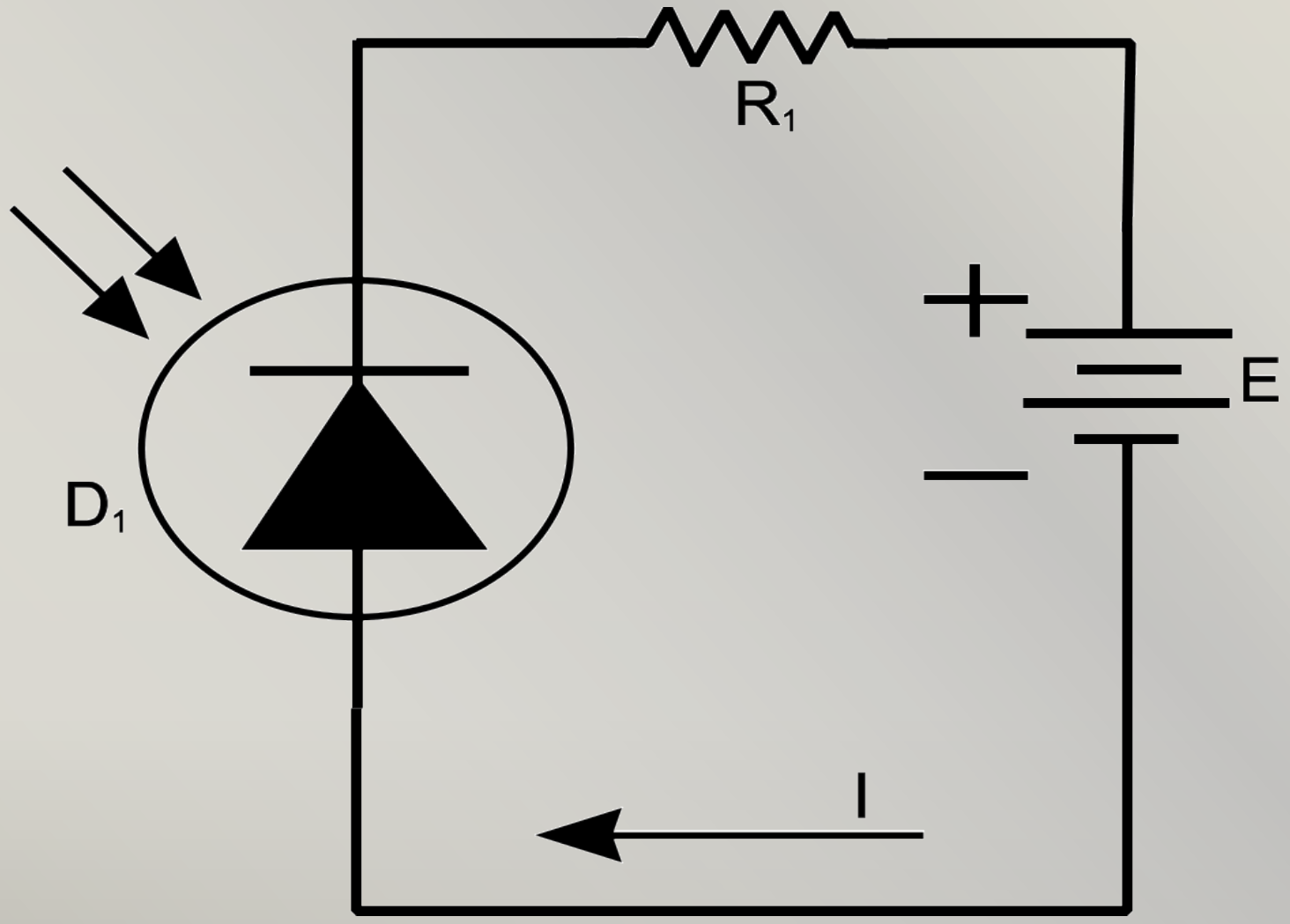
1) To show that current through a photodiode increases as the light falling on the device increases.
2) To verify that current through a phototransistor varies with varying light

Introduction

- We have seen in a previous experiment that the resistance of both a photodiode and a phototransistor changes as the intensity of the light hitting the device varies.

- Today we will continue studying these important devices by measuring the current characteristics under various light conditions
- The diagram on the next slide shows a properly biased photodiode.
  - Note: The polarity of the voltage source is such that the photodiode is reversed biased.

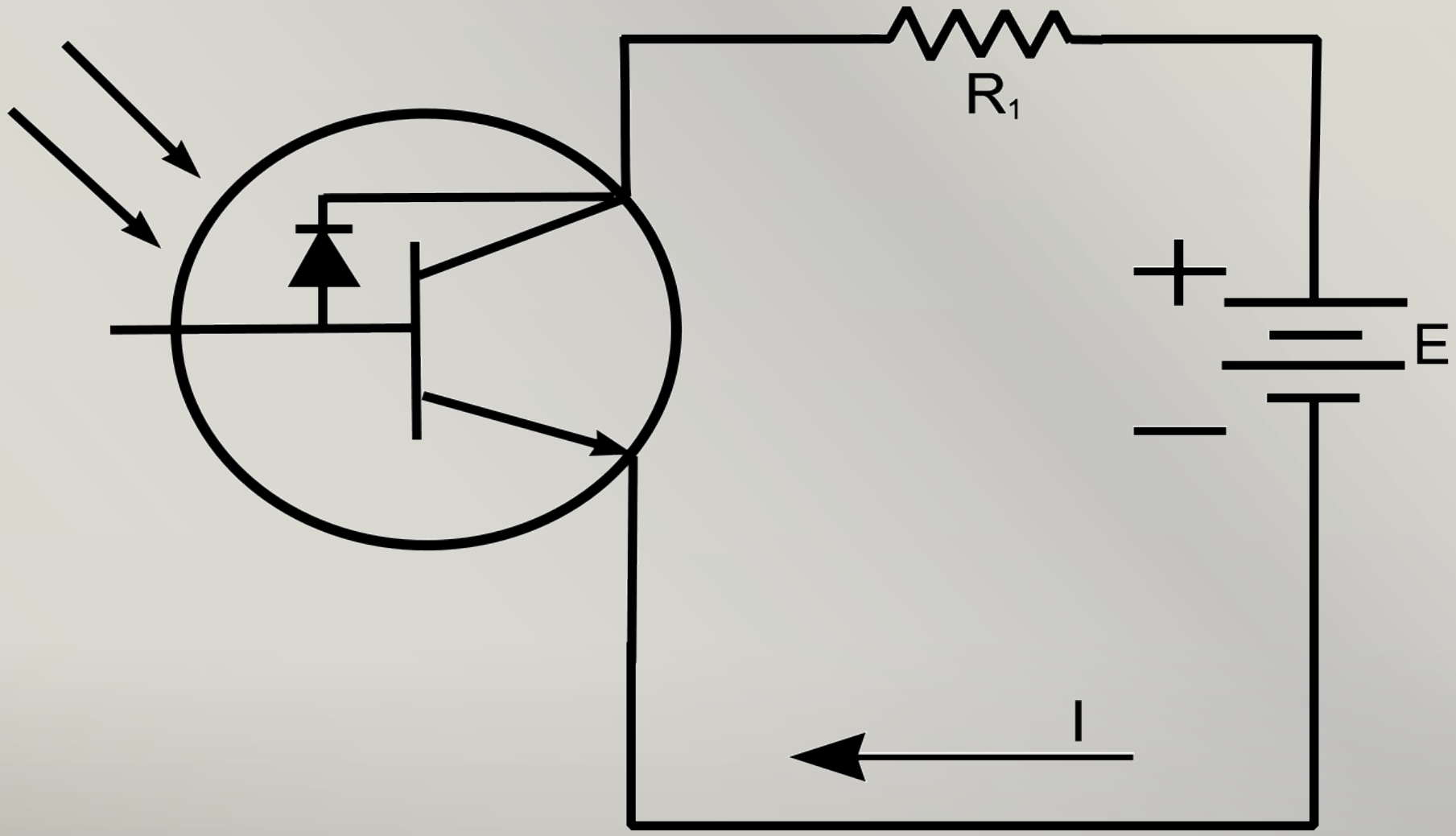
Properly Biased Photodiode



Properly Biased Phototransistor

- A similar situation exists in the circuit on the next slide, which shows a properly biased phototransistor
- Note the base and collector are still reverse-biased with this arrangement
- The collector-base junction is reverse-biased as well

Properly Biased Phototransistor



- The photodiode resistance will change as the light changes, causing the base current to change as well
- This changing current will be amplified by the transistor, resulting in a change in collector current
- The current gain of the transistor is the reason the current carrying capability of the phototransistor in generally much larger than that of the photodiode alone

Procedure

- In this experiment, you will be using the same phototransistor you used in the last experiment
- Photodiode measurements will be made between the base and collector terminals of the device

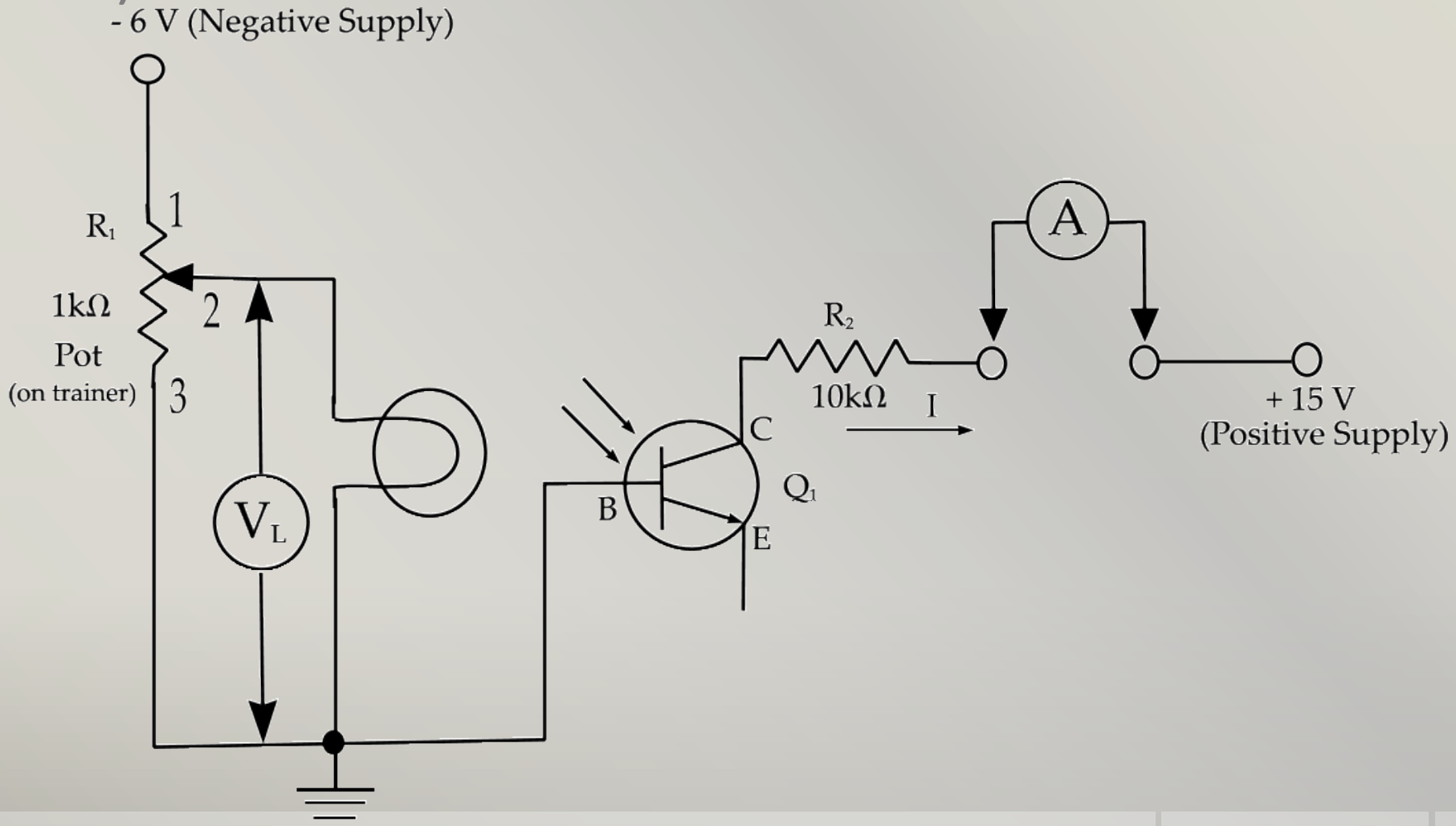
- Phototransistor measurements will be made between the collector and emitter terminals of the device
- We will be using a small lamp as a light source.
  - The lamp will be set at a fixed distance from the transistor
  - By varying the lamp voltage, we can change its brightness and observe how the photodiode and phototransistor currents vary

1. Before constructing the circuit, turn the power supply on and set the positive supply to + 15V and set the negative supply to – 6V. *Be careful not to change these settings throughout the experiment!*
2. *Mount the phototransistor on the breadboard as shown on the slide after next*
    a) *Carefully bend the leads at a 90° so the device points horizontally*

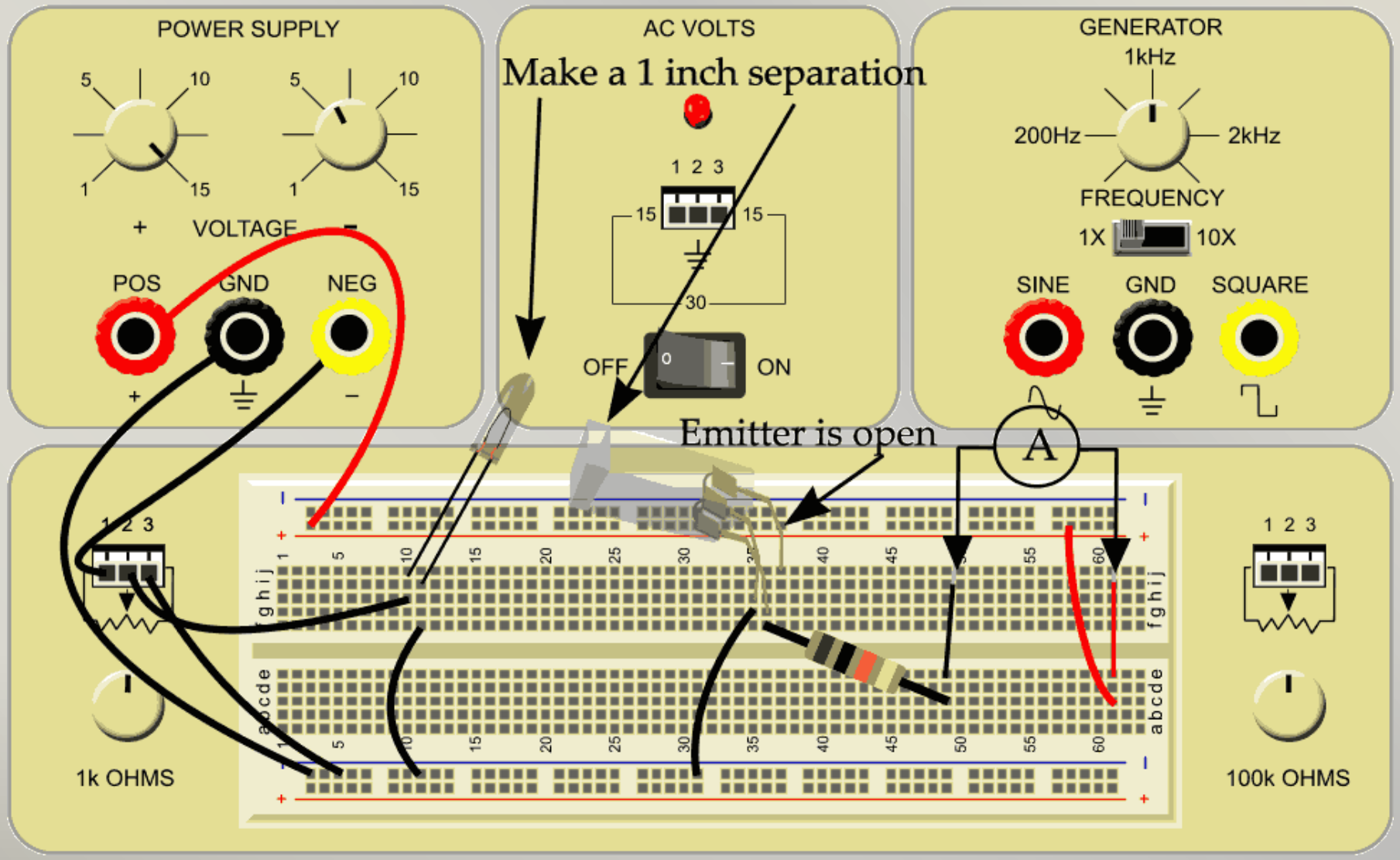
3. Mount the lamp on the breadboard about 1 inch from the transistor
    a) Depending on the type of lamp supplied, you may have to solder leads onto the lamp or socket before mounting it to the breadboard
4. With the power off, construct the circuit shown on the following slide
    a) The base lead is to be connected to ground

b) The collector lead is to be connected to R_2

c) Note: The emitter lead is left unconnected



Photodiode Measurement Ckt



5. Switch your meter to the 50❍✌ range and connect it in series as shown on the schematic and in the pictorial.

6. Turn on the power and set R_1 so that the lamp is off.

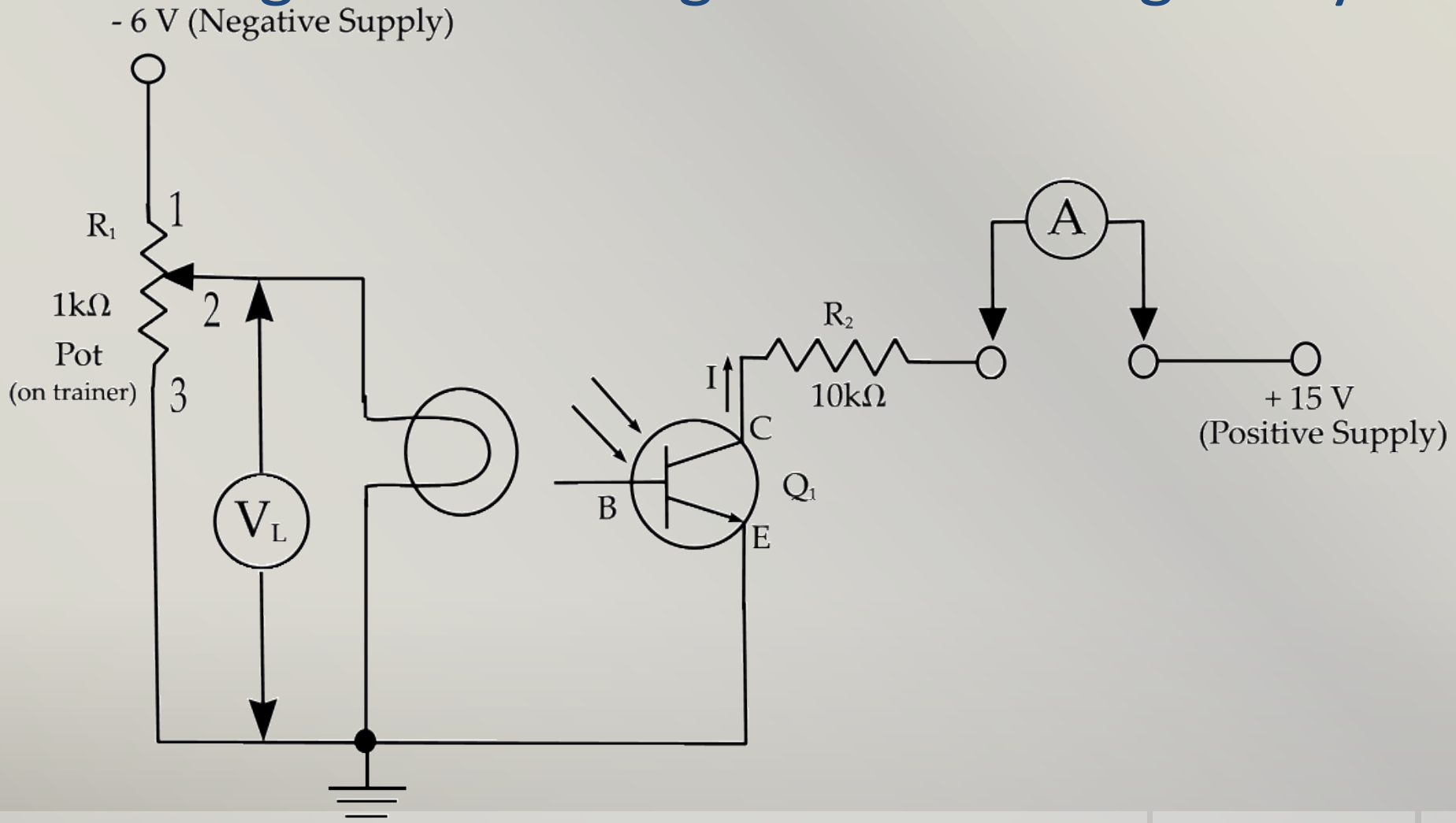
   a) Measure the current through the photodiode and record the voltage in the table on the following slide

Data Table for Experiment 6

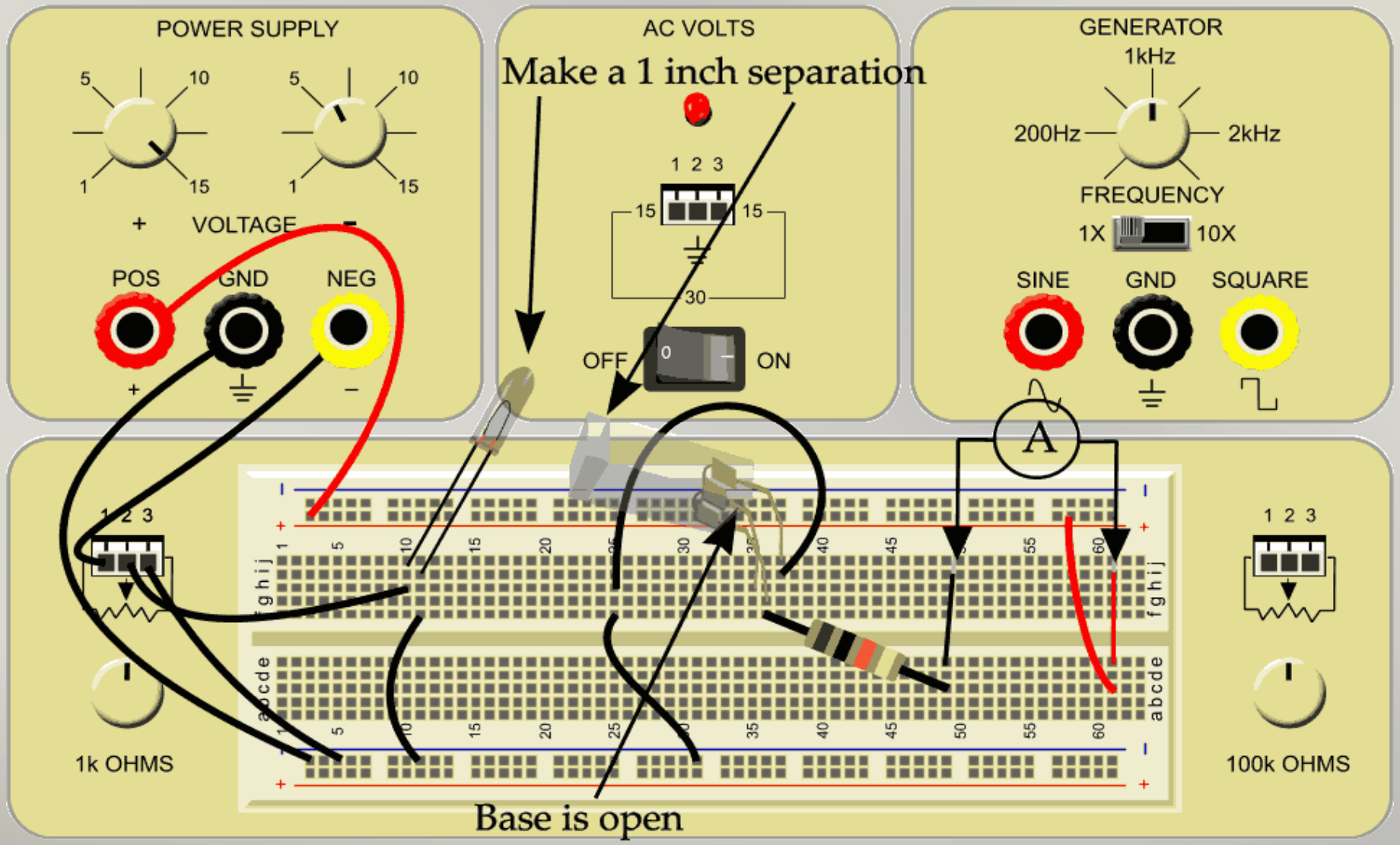
Lamp Voltage	Photodiode Current	Phototransistor Current
0 V		
-1 V		
-2 V		
-3 V		
-4 V		
-5 V		
-6 V		

7. Using your volt meter, set voltage on the meter across the lamp to 1 V
    a) Replace meter with a jumper
    b) Set meter to the 10 VDC range to measure the voltage across the lamp
8. Return the meter to measure the current again and place the value in the data table
9. Continue with each of the lamp voltages in the table and measure & record the current for each in the data table

10. Turn off the power and modify the circuit using the following schematic to guide you



Phototransistor Measurement Ckt



11. Turn on the power and repeat all the measurements for the various lamp voltages in the data table and set your meter to the 2.5 mA range
    a) Mark the results in the table
12. Our results can be seen on the following slides

Results

- Your results should be similar to ours, but don’t worry if there are some discrepancies.
  - Variations in lamp output, distance, and photodiode and phototransistor characteristics can all contribute to experimental error

Data table with CIE Results

Lamp Voltage	Photodiode Current	Phototransistor Current
0 V	0	5μA
-1 V	5μA	100μA
-2 V	20μA	250μA
-3 V	25μA	400μA
-4 V	27μA	600μA
-5 V	35μA	1.2mA
-6 V	40μA	1.45mA

- However; you should see the same general trend.
  - As the lamp intensity increased, the current should have increased as well, because of the decreased resistance
- The phototransistor current should have been much greater than the photodiode current.
  - This is because of the current gain of the transistor

Final Discussion

- You measured both the photodiode and the phototransistor characteristics.
  - With each of these devices, the current increased as the light increased
- The photodiode was measured by using the base and collector leads of the phototransistor

- The phototransistor measurements were made between the emitter and collector leads of the this transistor
  - This is the normal operating mode for a phototransistor, although you'll often see additional base bias applied through an external resistor

- To make the results repeatable, we used a standard lamp to provide the light for the phototransistors.
  - However, because of component tolerances or differences, a wide range of variations from device to device is to be expected
  - Your results probably were not linear, in that the current did not increase as much as the lamp voltage did.

- Not only is the phototransistor itself less than perfect, but the intensity of the lamp probably didn't increase linearly with changes in lamp voltage either; all of which would affect the results.

- Phototransistors are often used as discrete devices, but they will be found combined with other components in some applications.

Questions?

Resources

- Rosenow. (2001). *Lesson 1452: Optoelectronics*. Cleveland: Cleveland Institute of Electronics.

The End

Developed and Produced by the Instructors in the CIE Instruction Department.